USB4™ Cable Electricals and System Design

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USB Developer Days 2019 – Taipei, Taiwan

November 20, 2019

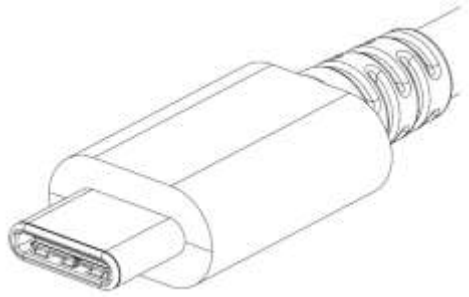
Agenda

- Cable Electricals
  - Electrical Spec
    - Cables
    - Mated Connectors
  - Design Challenges
  - Compliance Test
- System Design Guidelines
  - Electrical Design Considerations
  - Physical Design Considerations
    - Trace geometries
    - Routing practices, vias, and component placements
    - Layout design
  - Component selection

Cable Electricals

Yun Ling,
Sr. Principal Engineer, Intel

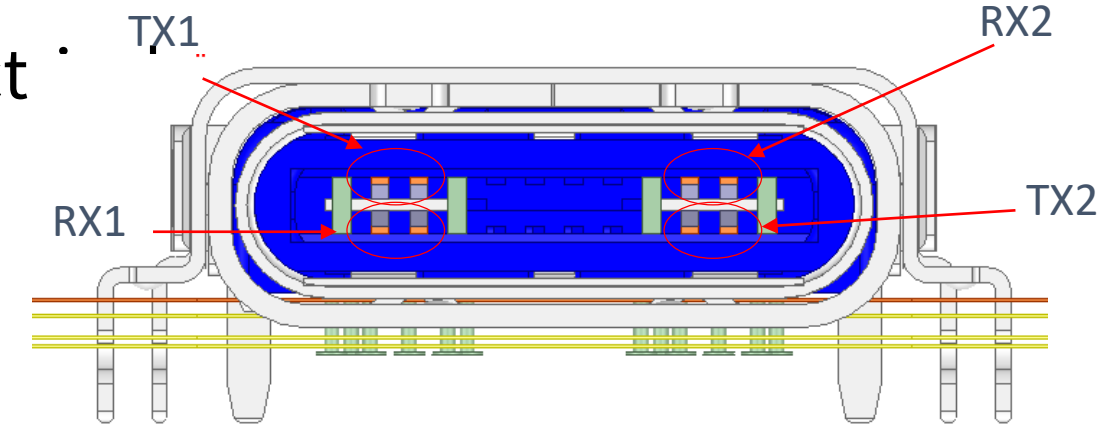
USB Type-C® Cables and Connectors



Looking into the product receptacle:

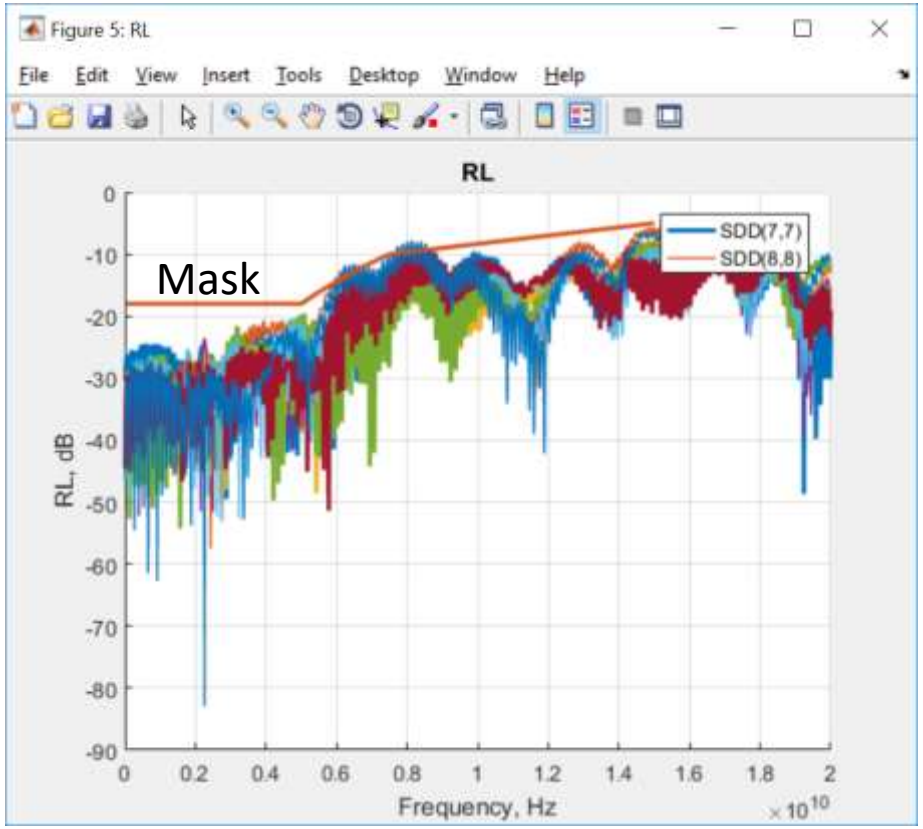
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	Vbus	CC1	D+	D−	SBU1	Vbus	RX2−	RX2+	GND
GND	RX1+	RX1−	Vbus	SBU2	D−	D+	CC2	Vbus	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

- Focus on C-to-C cable high speed elect
- No change to mechanical spec



USB4™ Gen2 Cable Spec

- USB4 Gen2 cable electrical spec is identical to USB3.2!
  - It uses the same integrated S-parameters, avoiding the S-parameter mask as much as possible.
- Key spec items include:
  - Insertion Loss Fit at Nyquist
  - Integrated Multi-Reflection
  - Integrated Return Loss
  - Integrated Crosstalk



S-parameter mask-based spec creates too many false failure cases!

Insertion Loss Fit and Multi-Reflection

- Insertion loss, IL(f), represents the remaining signal after it travels thru the cable.
- IL(f) may be decomposed into Insertion loss fit, IL_fit(f) and multi-reflection, MR(f).
  - IL_fit: uses a smooth function to fit the IL, representing the signal.
  - MR = IL – IL_fit, representing the multi-reflection noise.
- IL fit at Nyquist frequency = IL_fit (Nyquist frequency):

USB4 Gen2 or USB 3.2 Gen2:

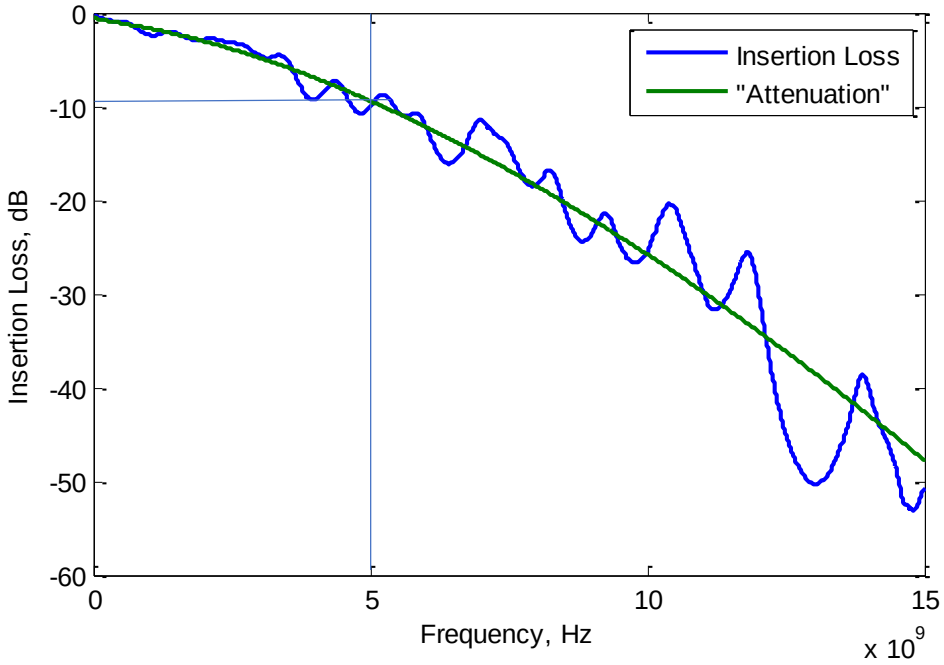
$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

USB4 Gen3:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3} + e * \sqrt{f^4}$$

Added a f^2 term to make the fitting more robust

ILfitatNq



System loss budget

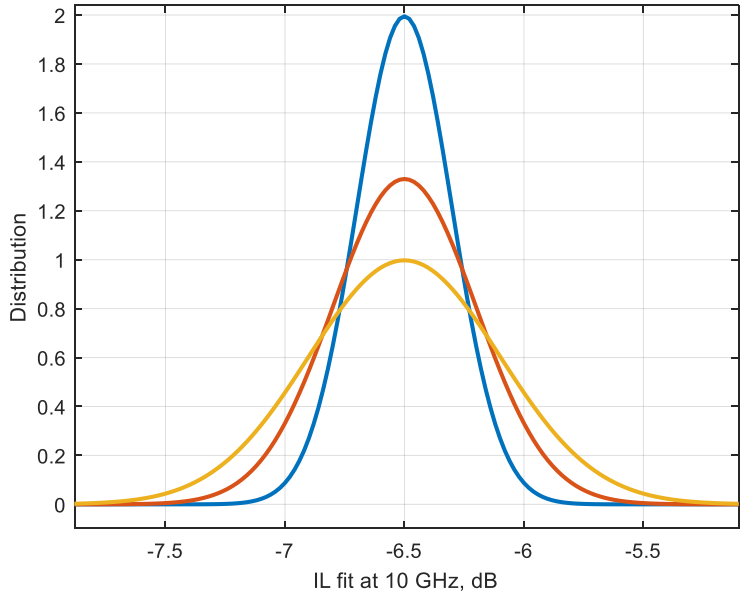
- Host/device loss includes everything in the signal path from die to connector tongue.
- USB4 Gen2 supports a 12 dB (2m) cable while USB3.2 Gen2 support only a 6 dB (1m) cable due to the difference in system loss budget.
- Host/device loss budgets are informative only.

	Host	Cable	Device	Total
USB3.2 Gen2 (10 Gbps)	8.5 dB	6 dB	8.5 dB	23 dB
USB4 Gen2 (10 Gbps)	5.5 dB	12 dB	5.5 dB	23 dB
USB4 Gen3 (20 Gbps)	7.5 dB	7.5 dB	7.5 dB	23 dB

Insertion Loss Fit Spec

- USB 3.2 Gen2
  - ≥ −4 dB at 2.5 GHz
  - ≥ −6 dB at 5 GHz
  - ≥ −11 dB at 10 GHz
- USB4 Gen2 (2m)
  - ≥ −7.0 dB at 2.5 GHz
  - > −12 dB at 5 GHz

- USB4 Gen3
  - ≥ −1 dB at 100 MHz
  - ≥ −4.2 dB at 2.5 GHz
  - ≥ −6 dB at 5 GHz
  - ≥ −7.5 dB at 10 GHz
  - ≥ −9.3 dB at 12.5 GHz
  - ≥ −11 dB at 15 GHz



- Cable length mentioned in the spec is for reference only. Performance spec dictates cable length.
- Consideration to HVM variation is a must!
  - Spec is meant for the worst-case, not the mean value. For example, to meet the ≥ −7.5 dB IL_fit_at_10GHz spec, the mean has to be significantly > −7.5 dB to account for HVM variation

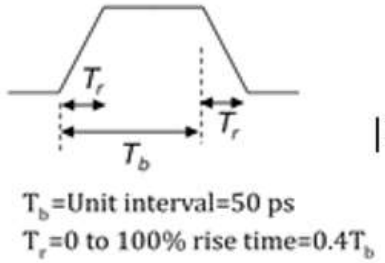
Integrated Multi-Reflection Spec

Multi-reflection

Input signal pulse frequency spectrum

$$IMR = dB\left(\sqrt{\frac{\int_0^{f_{max}} |MR(f)|^2 |Vin(f)|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

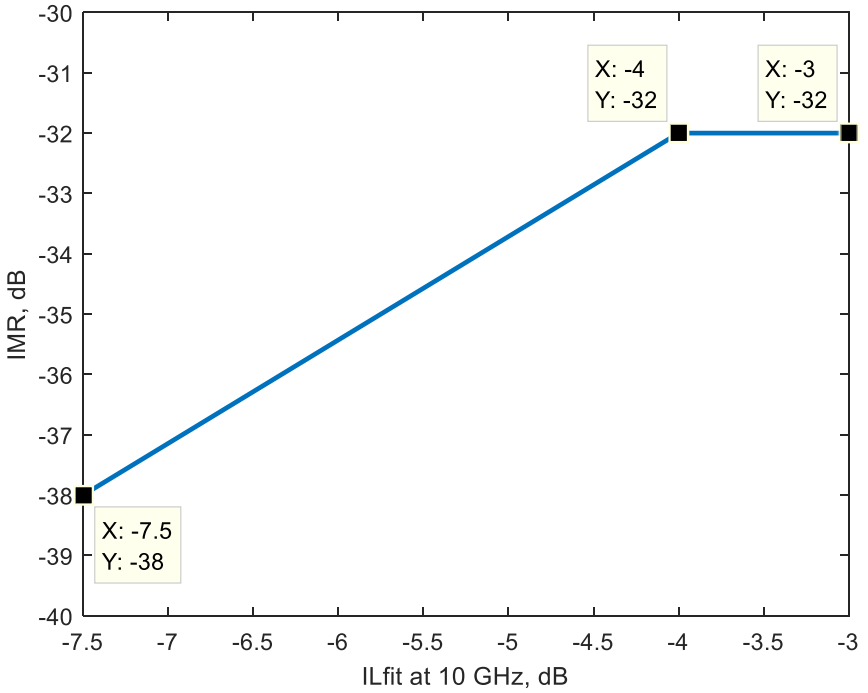
Normalization factor



$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

fmax=12.5 for USB4 Gen 2 and 20 GHz for USB4 Gen3
Tb=Unit Interval, 100 ps for USB4 Gen2 and 50 ps for USB4 Gen3

- IMR is normative for USB4 Gen2
- IMR is *informative* for USB4 Gen3
  - A larger IMR is allowed if cable loss is smaller

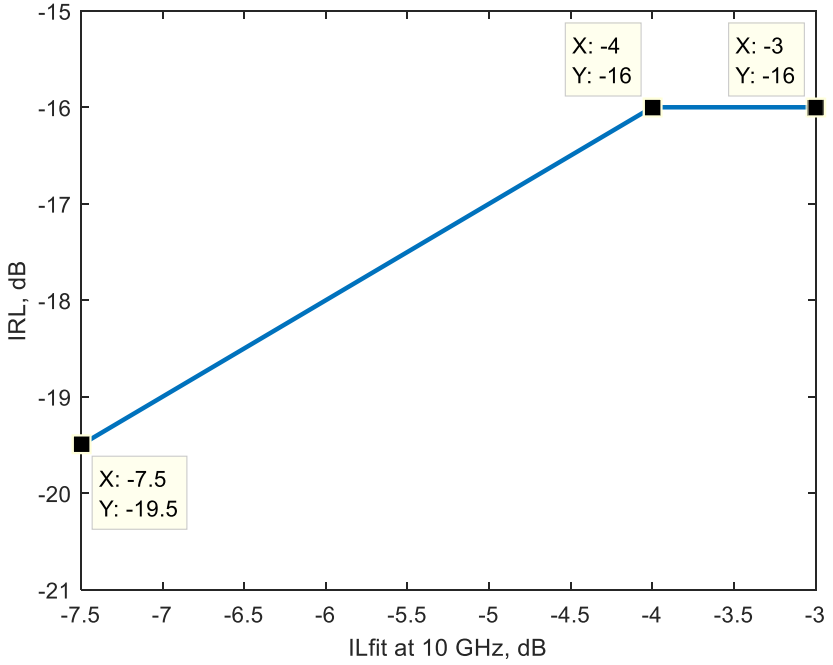


Integrated Return Loss

$$IRL = dB\left(\sqrt{\frac{\int_0^{fmax}|Vin(f)|^2|SDD21(f)|^2(|SDD11(f)|^2+|SDD22(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

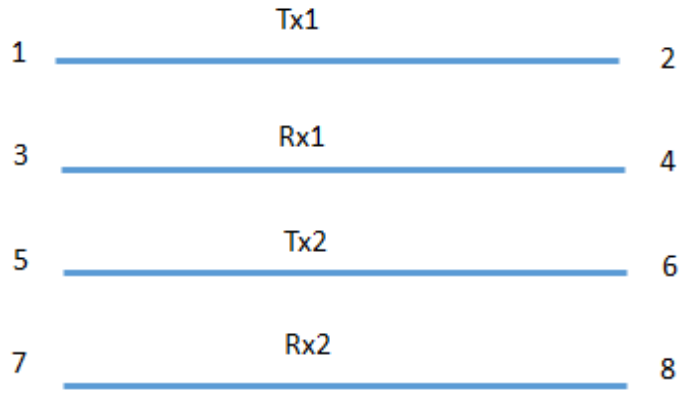
Integrated Return Loss measures the undesired interaction/reflection between the cable and host/device.

- IRL is a normative requirement.
- More IRL is allowed if cable loss is smaller



Integrated Crosstalk

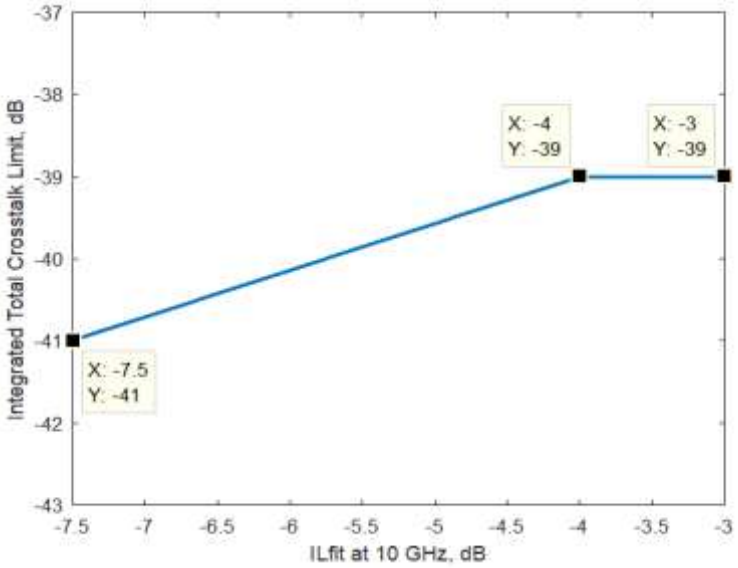
$$\text{IXTi\_DP or IXTi\_USB} = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 \sum_j |SDDij|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$



i=victim; j=aggressor

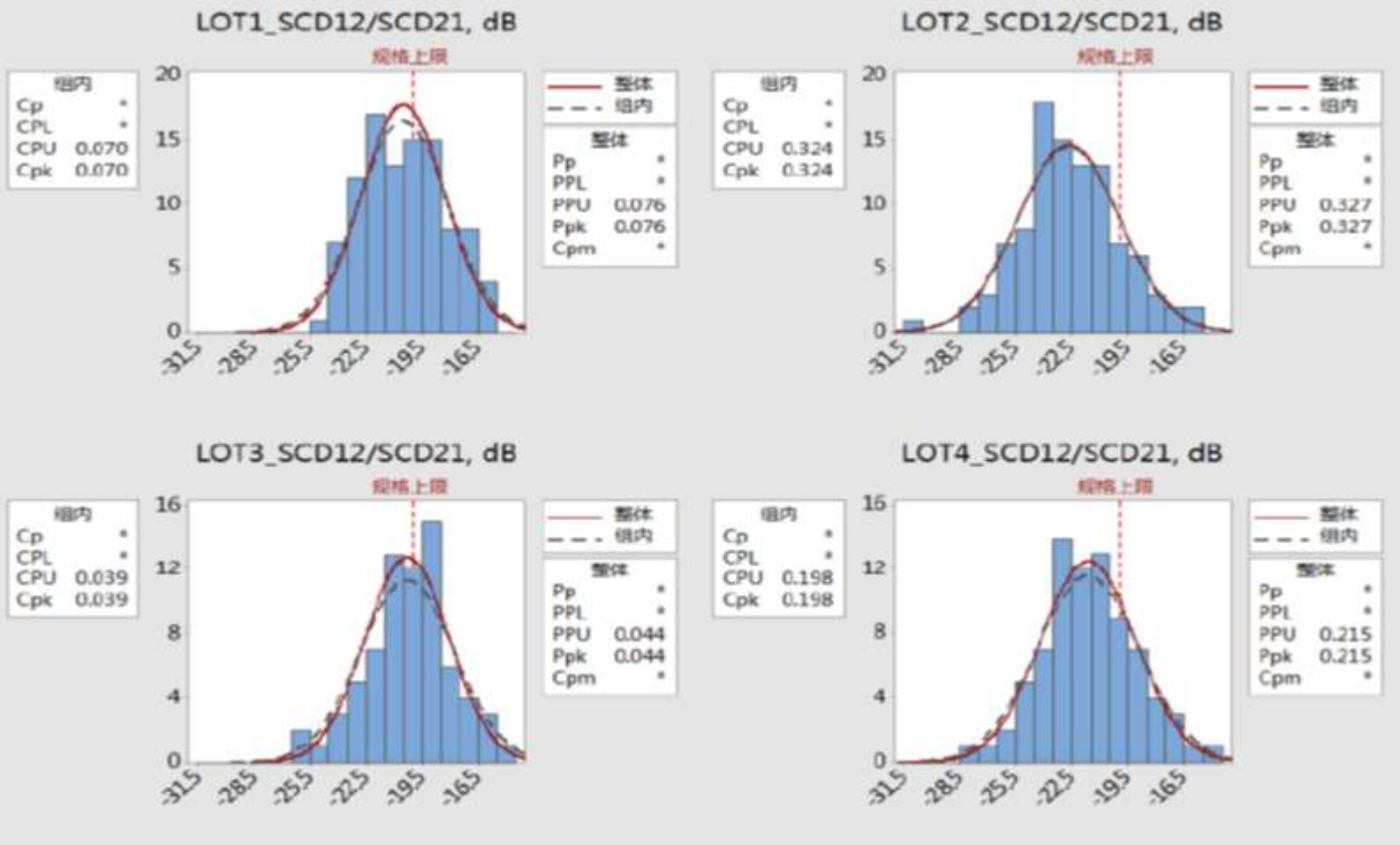
IXT_DP				IXT_USB			
i	j			i	j		
1	4	6	8	1	3	7	6
2	3	5	7	2	4	8	5
3	2	6	8	3	1	5	8
4	1	5	7	4	2	6	7
5	2	4	8	5	3	7	2
6	1	3	7	6	4	8	1
7	2	4	6	7	1	5	4
8	1	3	5	8	2	6	3

- USB4 Gen3 specifies the combined total crosstalk in USB mode and DP alt-mode.
  - USB mode: 2 NEXT +1 FEXT
  - DP mode: 3 FEXT
- It is a better way to control crosstalk as compared to specify crosstalk between each pairs.
  - Easier to meet the spec for the same effect



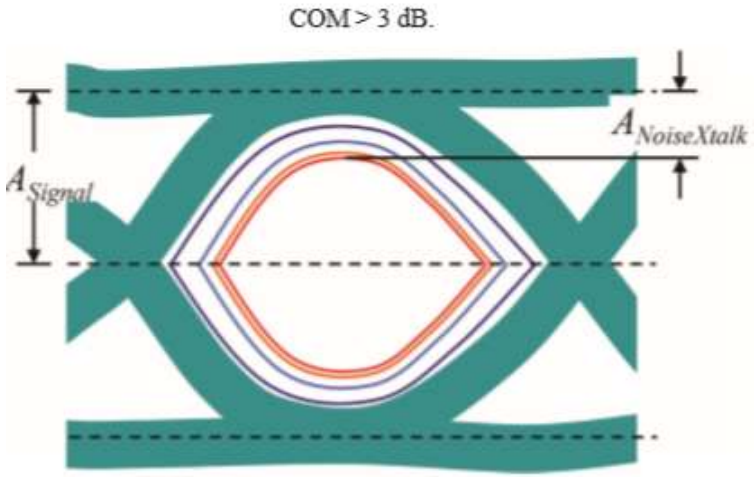
Mode Conversion

- Mode conversion is relaxed from -20 dB to -17 dB (to 10 GHz) for USB4 Gen3 due to industry capability reality



COM – Channel Operation Margin

- COM is a figure of merit to measure channel electrical quality defined by IEEE 802.3. It is a Signal-to-Noise Ratio developed in a similar way to Statistical Analysis
- Collaterals needed to calculate COM:
  - Measured cable S-parameters
  - Reference hosts/devices
  - Reference Tx/Rx termination
  - COM configuration file



Spec Tx jitter

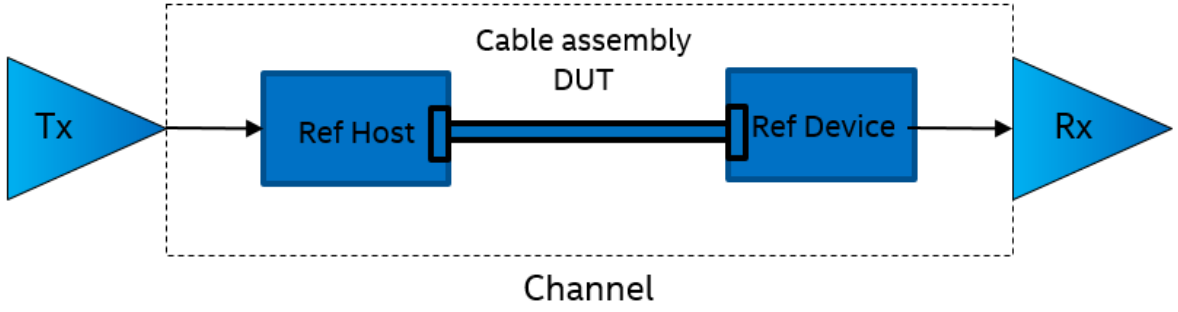
Spec Tx Equalizer

Ref Tx Termination

$$COM = 20 \log \frac{A_{Signal}}{A_{NoiseXtalk}}$$

Spec Rx Equalizer

Ref Rx Termination

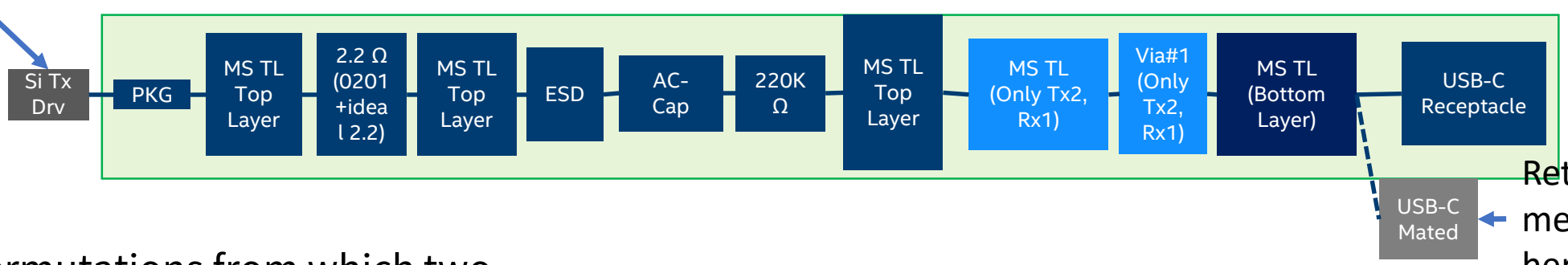


Reference Host – 1/2

- Topology of the Reference Host/device

Die model is used for collection of Insertion Loss and Return Loss. But it is not in the reference host

Components of Reference Host Model



- Variables permutations from which two reference hosts are selected
  - Impedance of traces
  - Attenuation of traces
  - Trace length
  - Location of the ESD

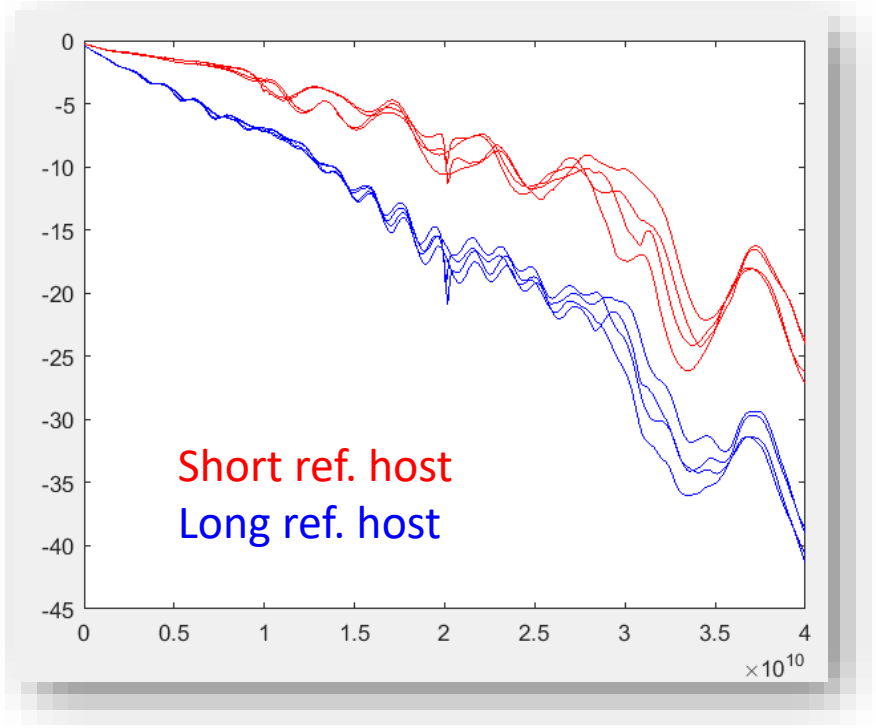
Two reference hosts/devices are defined:
long host/device and short host/device.

Long host/device has about -7.5 dB loss at 10 GHz (with die-loading)

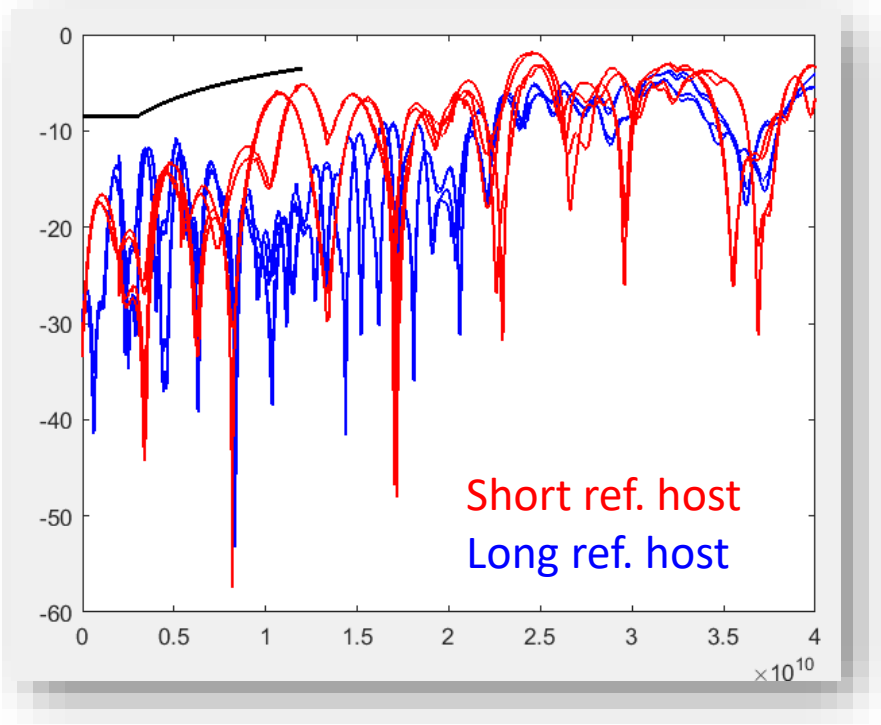
Short host/device has the minimum loss possible

Reference Host – 2/2

- Insertion loss up to receptacle's tongue include die load



- Return loss at TP2 (w/ die load attached)



COM Config File for USB4™ Gen3

- All equalization settings are based on the USB4 Specification.
  - Tx FFE
  - RX CTLE and DFE
- Tx random jitter and deterministic jitter are derived from the USB4 specification.
- The input voltage swing (A_v, A_fe, and A_ne) is assumed to be the typical range of 0.8 to 1.2 V (differential peak-to-peak)

Parameter	Setting	Unit	Information
f_b	20	GBd	USB4 Gen 3 data rate
C_d	[0 0]	nF	Tx and Rx capacitive loading. It is set to zeros as the die-loading is treated as part of the channel
R_d	[42.5 42.5]	Ohm	Tx and Rx termination resistance
ffe_preset	Table 3-4 of USB4 Specification		Tx equalization presets
g_DC	[-9:1:0]	dB	CTLE DC gain
f_p1	5	GHz	CTLE pole 1
f_p2	10	GHz	CTLE pole 2
f_z	3.55	GHz	CTLE zero
A_v	0.4	V	Signal swing
A_fe	0.4	V	FEXT aggressor swing
A_ne	0.6	V	NEXT aggressor swing
N_b	1		Number of DFE tap
b_max(1)	0.7		DFE bound, ratio to cursor
Sigma_RJ	0.01	UI	Tx ramdom jitter, rms.
A_DD	0.085	UI	Tx deterministic jitter, mean-to-peak
DER_0	1e-12		Target raw bit-error-rate
eta_0	3.3e-8	V^2/GHz	One sided noise spectral density
SNR_TX	40	dB	Tx signal to noise ratio
COM Threshold	3	dB	Pass/fail criterion

Spec Validation

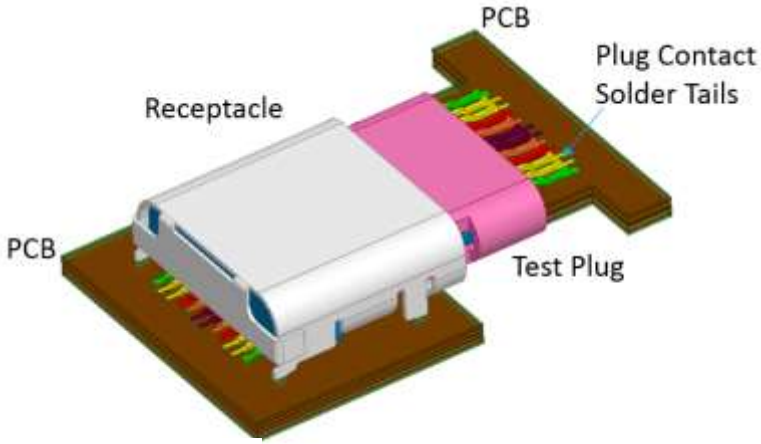
- Spec cables: “worst-case” cables that hit the spec limits at various ILfit @10 GHz.
  - The spec cables marginally pass/fail COM

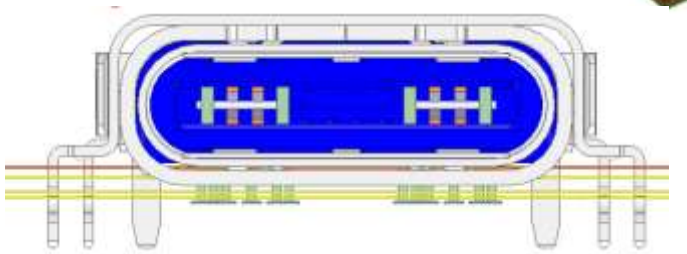
- Measured cables: measured TBT3 cables from different vendors
  - Almost all known TBT3 cables pass the integrated parameter and COM spec.

Host#	Device#	Cable#	Victim	ILfitatNq	Signal_mV	ISI_mV	Crosstalk_	COM	COM Limit	Pass/Fail	Integrated Parameter
1	1	Spec long cable	Tx2	-22.9182	47.53322	20.7	7.86	2.925708	3	Fail	Border Line
2	2	Spec short cable	Tx2	-11.0043	142.7662	72.44	17.72	2.936699	3	Fail	Border Line
1	1	Measured Cable25	Tx2	-21.2287	53.99262	21.53	6.62	3.862656	3	Pass	Pass
1	2	Measured Cable26	Rx1	-17.7044	76.09064	28.88	21.9	2.681497	3	Fail	Fail IXT
1	1	Measured Cable27	Tx2	-22.2626	50.48604	21.25	6.17	3.528888	3	Pass	Pass
1	1	Measured Cable29	Rx1	-22.7136	49.78228	21.08	5.83	3.45617	3	Pass	Pass
1	1	Measured Cable30	Tx2	-21.4544	54.79757	22.36	7.8	3.683021	3	Pass	Pass
1	1	Measured Cable31	Rx1	-21.2108	53.77911	23.54	6.63	3.375939	3	Pass	Pass
1	1	Measured Cable33	Tx2	-22.299	49.82818	22.82	5.46	3.150423	3	Pass	Pass
1	1	Measured Cable32	Tx2	-19.5524	66.52476	33.3	12.65	2.522059	3	Fail	Fail IRL
1	1	Measured Cable22	Tx1	-19.9512	64.03106	28.25	10.45	3.248895	3	Pass	Marginal on IRL

Mated Connector Spec

- USB 3.2 and USB4 Gen 2 have only the informative receptacle/mated connector electrical spec.
- But for USB4 Gen3, the this is Normative.
- Need to define the “ Golden Plug”.

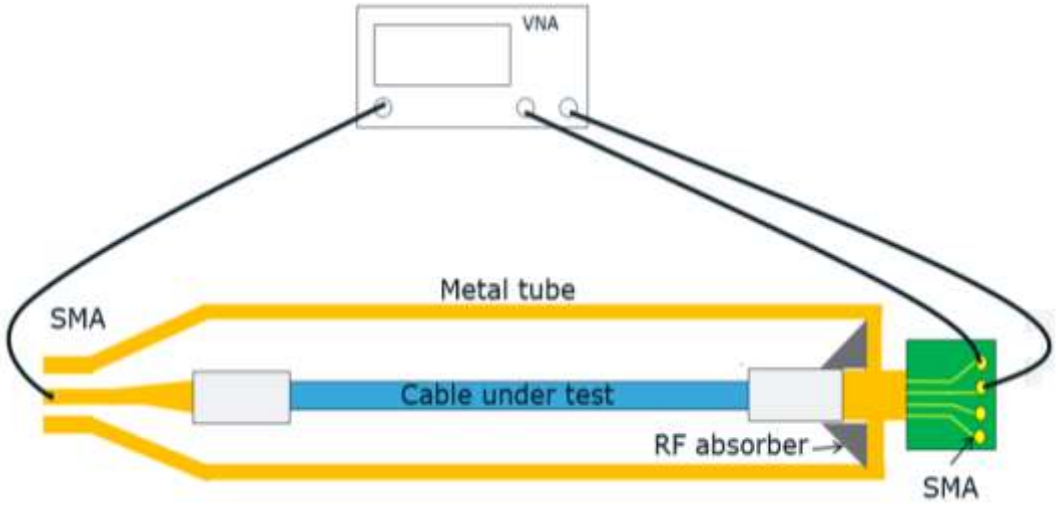


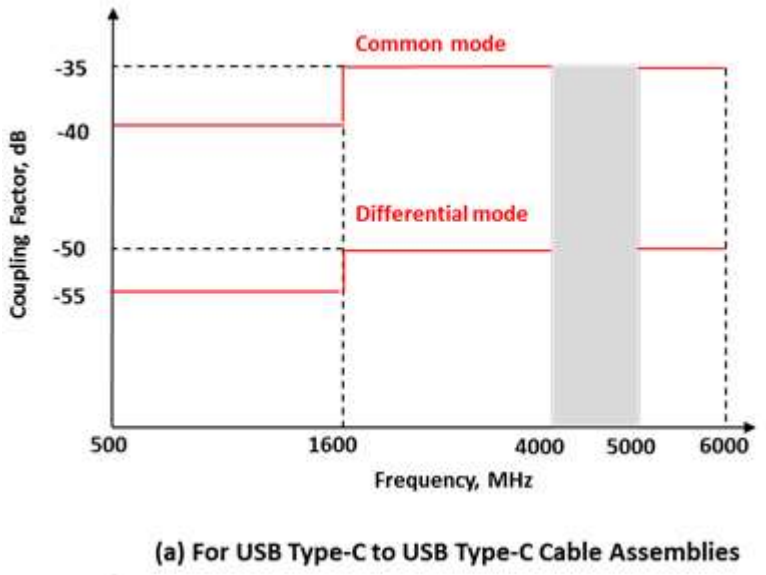


Parameter	Requirements
IL fit	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB at 5.0 GHz ≥ −1.0 dB @ 10 GHz ≥ −1.25 dB @ 12.5 GHz ≥ −1.5 dB @ 15 GHz5
IMR	≤ −39 dB
INEXT	≤ −43 dB
IFEXT	≤ −43 dB

Parameter	Requirements
IDDXT (Corsstalk between Tx/Rx and D+/D-)	≤ −50 dB
IRL	≤ −15 dB
SCD12/SCD21 (Mode Conversion)	≤ −20 dB (100 MHz to 10 GHz)

Cable Shielding Effectiveness



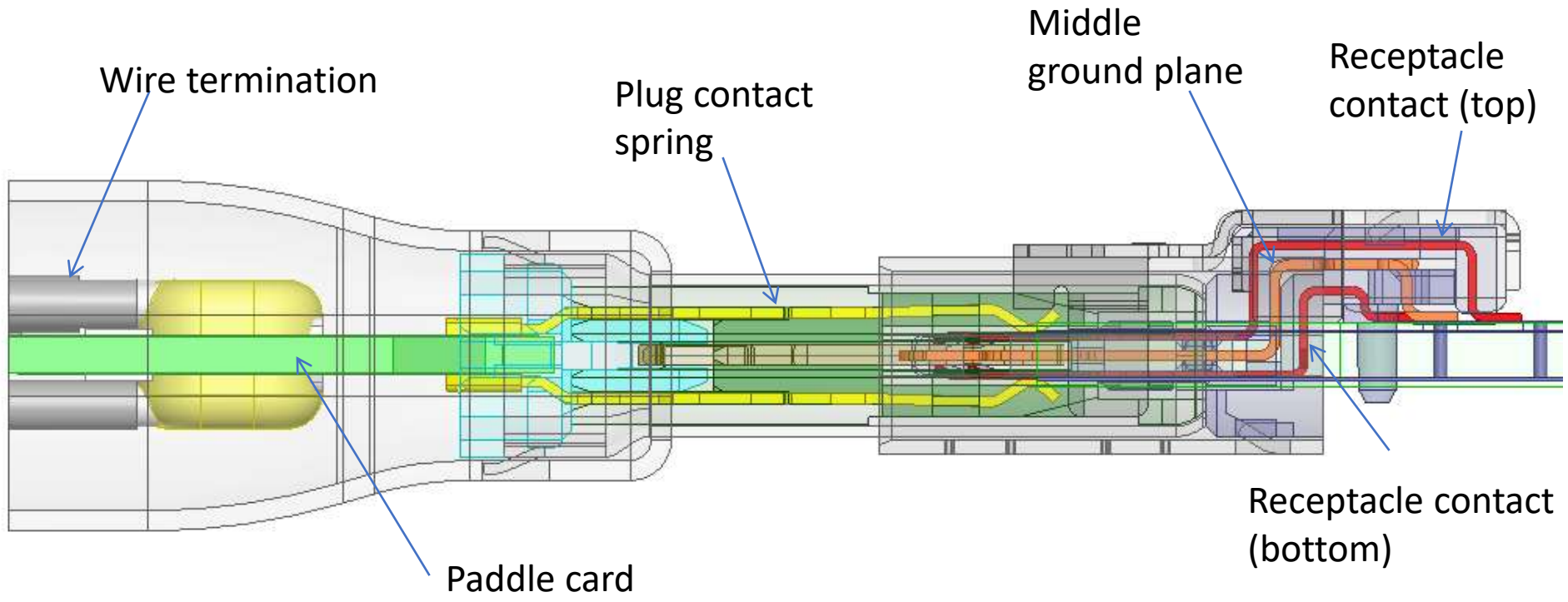


(a) For USB Type-C to USB Type-C Cable Assemblies

- The same shielding effectiveness requirement for USB 3.2 Type-C-to-Type-C cables is applicable for the USB4 cables.

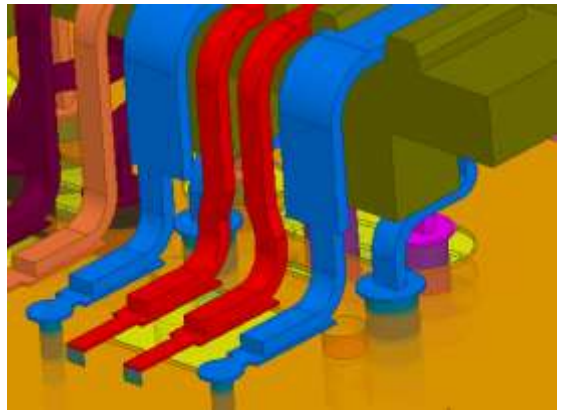
Design Challenges

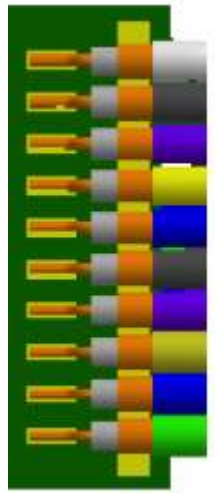
- USB4 Gen3 has tighter electrical requirements for cables and connectors.
- Everything along the signal path should be optimized.
  - *Loss, reflection, crosstalk*

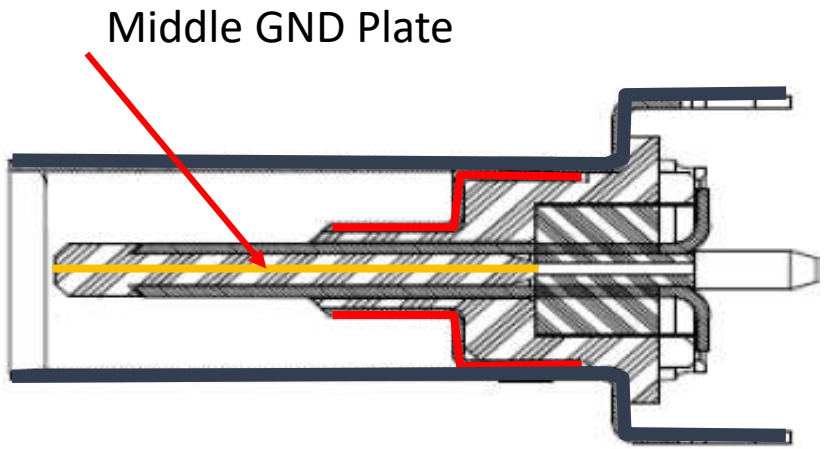


Design for Signal Integrity

- Raw cable – managing loss and skew
  - Loss per inch
  - Skew
  - Impedance
- Connector – minimizing discontinuities
  - Footprints
  - Contact geometries
  - Middle GND plates
- Paddle card – isolating coupling
  - Pin/wire-out
  - Footprints
  - Layer count
- Wire termination

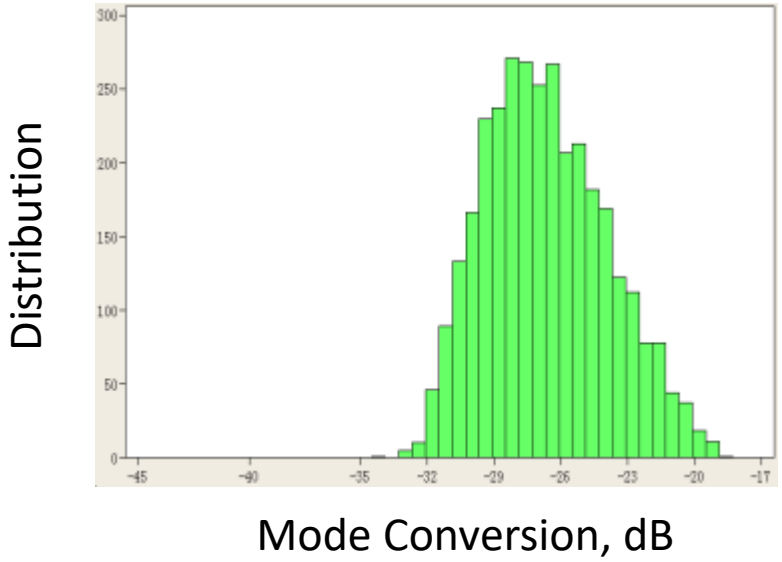


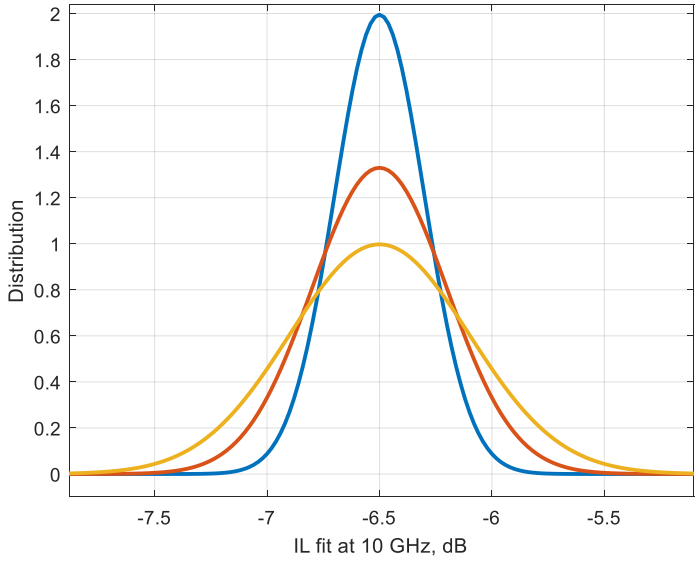




Compliance Test

- The USB4 Gen3 cable compliance spec is still under development.
- The goal is to have a robust cable/connector eco-system without prohibitive cost adders.
- Key challenges:
  - How to ensure the worst-case cable (within HVM limits) passes the spec?
  - How to check if a certified cable will continue to meet the spec?





USB4™ cable Spec Summary

- The main spec items for USB4 Gen3 cables are:
  - Insertion fit (normative)
  - IMR (informative)
  - IRL (normative)
  - IXT_USB/IXT_DP (normative)
  - COM (normative)
  - Mode conversion
  - Shielding effectiveness
- USB-IF will provide necessary supporting collaterals to extract/calculate the spec parameters
  - Tools and models
- The USB4 Cable/Connector Compliance Spec is still under development.

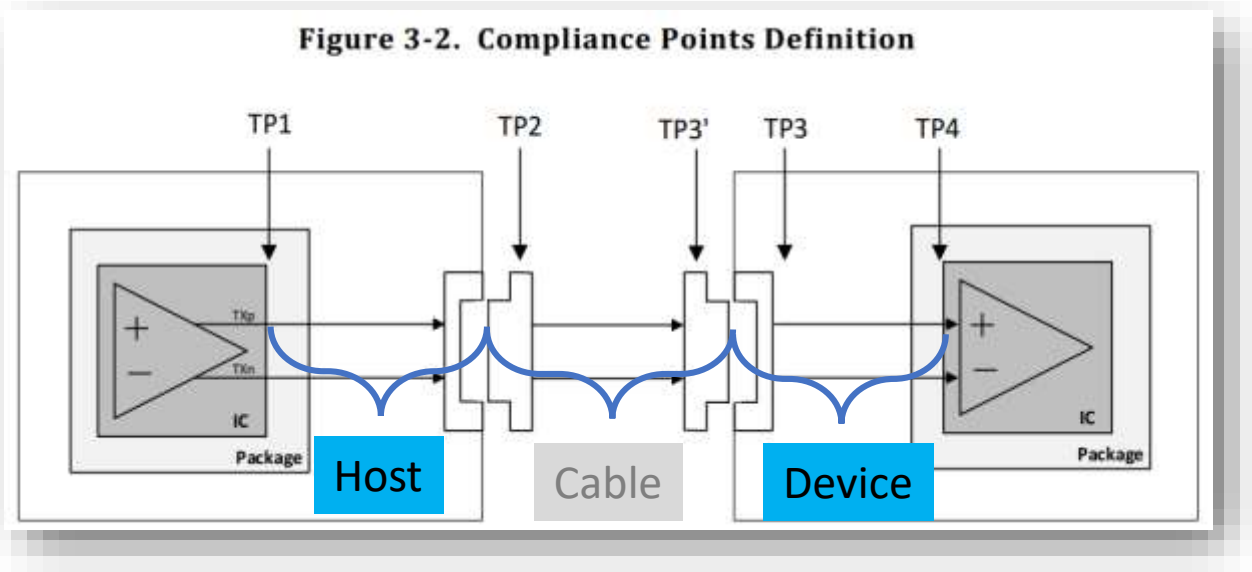
USB4™ System Design Guidelines

Reza Zamani *– Intel*

USB4™ System Design Guidelines

- Electrical Design Considerations
- Physical Design Considerations
  - Trace geometry
  - Routing practices, vias, and component placement
  - Layout design
- Component selection

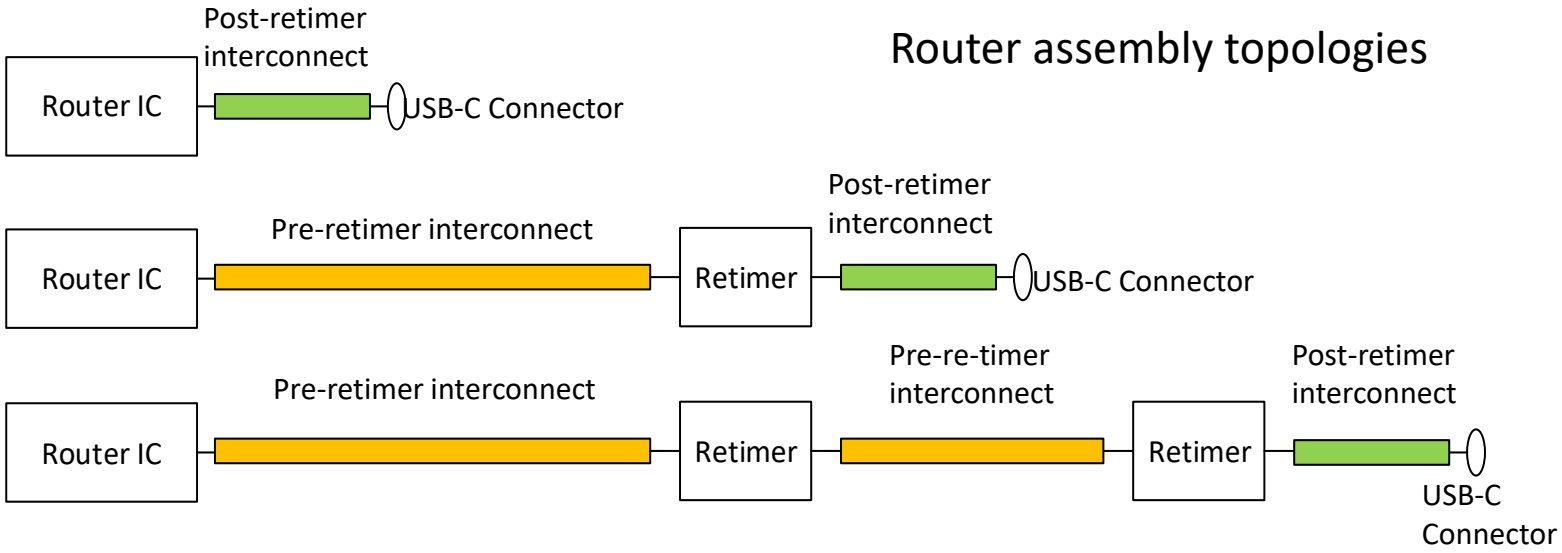
Host and Device Interconnects



- This presentation covers three categories of design considerations for the host and device interconnects/channels:
  1. **Electrical**
  2. **Physical/Layout**
  3. **Component selection and specifications**

Pre-Retimer and Post-Retimer Interconnects

- Various topologies of the router assembly is shown
- For this presentation, let's say we have two categories of interconnects. These have differences and demand potentially different design priorities. This presentation covers both



Pre-Retimer Interconnect	Post-Retimer Interconnect
• No explicit electrical/compliance target. Dependent on Tx and Rx PHYs at either ends. • Likely long => insertion loss becomes a design priority => PCB stack up selection, trace geometry optimization, etc. • Has fewer discrete components: AC-cap	• Explicit electrical/compliance design targets defined per the spec • Likely short => return loss becomes a design priority • Has more discrete components: AC-cap, ESD, bleed resistor, etc. => component selection, placement and routing are important

USB4™ System Design Guidelines

- **Electrical Design Considerations**
- Physical Design Considerations
  - Trace geometry
  - Routing practices, vias, and component placement
  - Layout design
- Component selection

Electrical Design Considerations

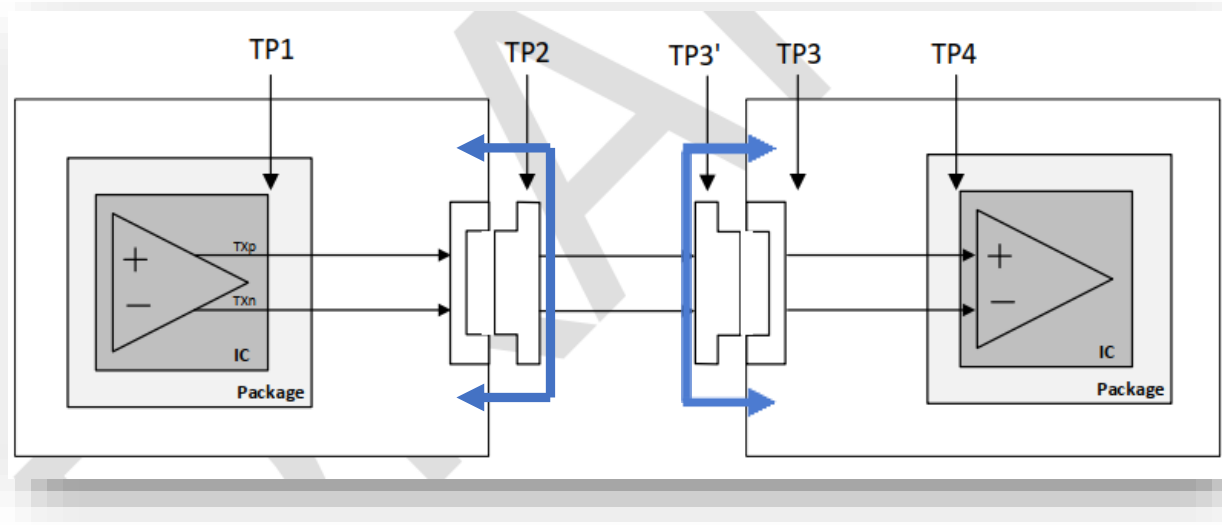
- **Insertion Loss:** The informative differential Insertion loss of the router assembly from the receptacle's tongue to the USB4 transceiver is limited to:
  - This includes the die load, IC package, PCB routing, discrete components, and receptacle's tongue
  - Note that the USB4 Gen2's host budget is smaller than USB3.2's. This is for supporting a 2m cable

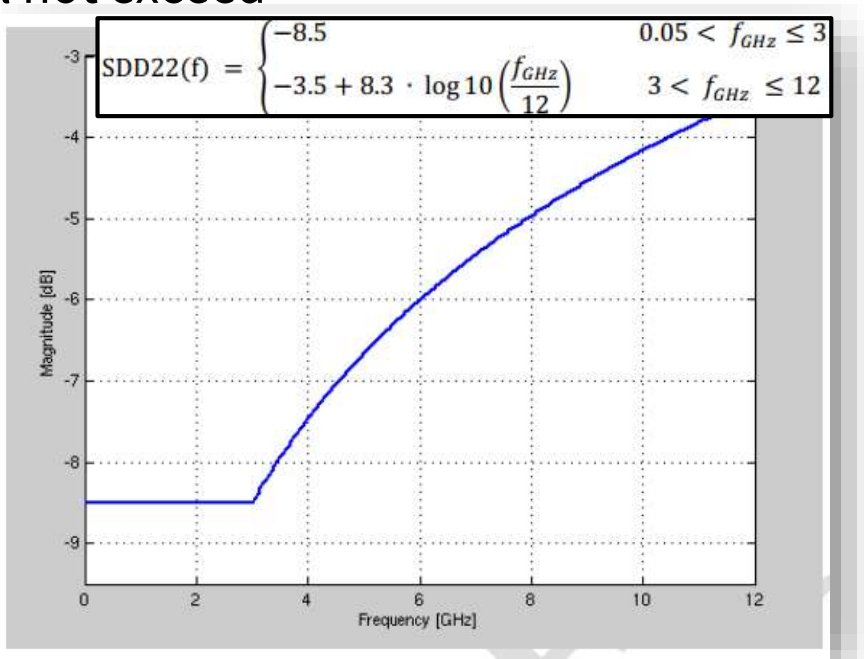
Router Assembly Support	***Informative* Insertion Loss Limit**
USB4 **Gen 3**	< **7.5 dB** at 10GHz
USB4 **Gen 2**	< **5.5 dB** at 5GHz
USB3.2	*< 8.5 dB at 5GHz*

- **Tx and Rx Compliance Tests:** The router assembly must meet Tx and Rx compliance. Even though performance of the silicon affects most of the compliance metrics, performance of the interconnect will impact the following
  - Tx and Rx return loss
  - Total Jitter (TJ) is impacted by the way of:
    1. Tx data dependent jitter (DDJ), which is impacted primarily by the insertion loss
    2. Cross talk in the interconnect contributes to Uncorrelated Deterministic Jitter (UDJ)
  - Rx stressed eye test (a.k.a. BER tolerance test)
  - Secondary effect on a few other compliance metrics, e.g. Tx AC Common mode voltage, etc.

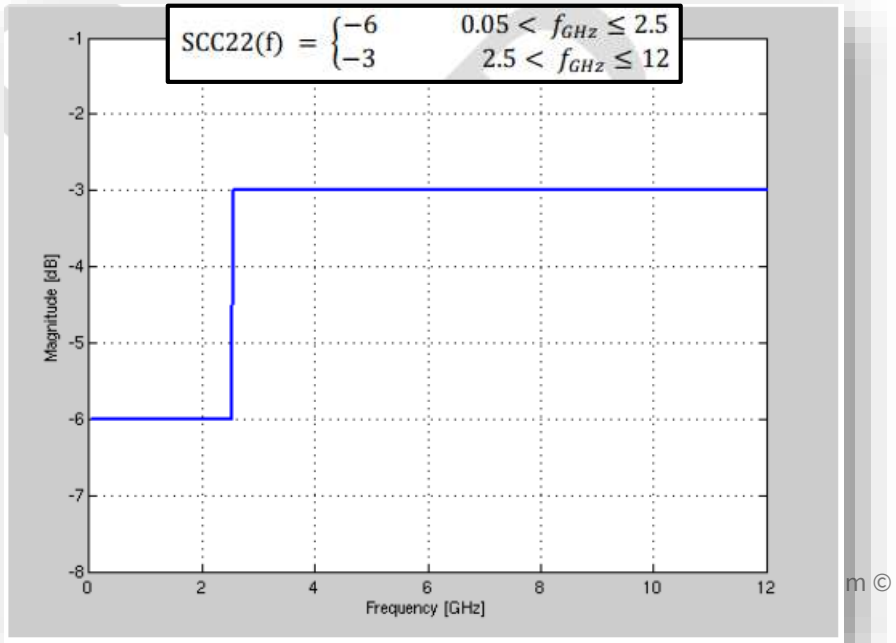
Return Loss Spec

- The Return loss spec defined at **TP2 for Tx** and **TP3' for Rx**
  - The necessary VNA measurements are collected with a compliance plug test board (See 3.3.6.1)
  - The measurement shall be referenced to single-ended impedance of 42.5 Ω
- The differential return loss **for both Tx and Rx** shall not exceed





- The common mode return loss **for both Tx and Rx** shall not exceed

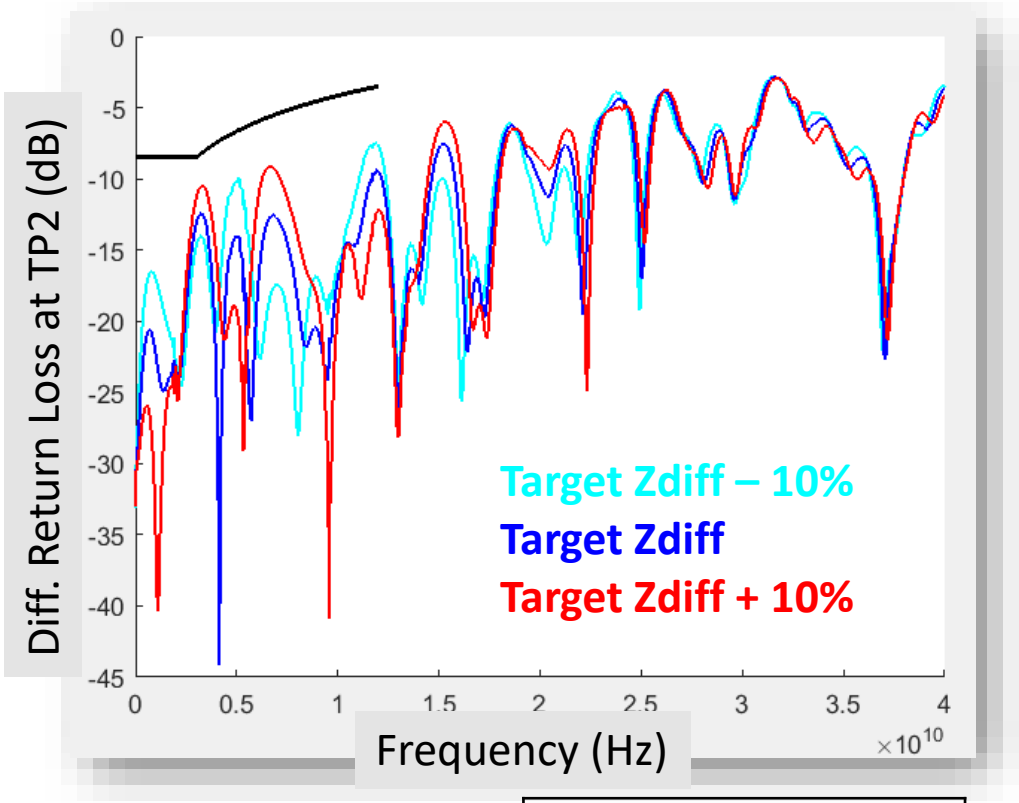


USB4™ System Design Guidelines

- Electrical Design Considerations
- **Physical Design Considerations**
  - **Trace geometry**
  - Routing practices, vias, and component placement
  - Layout design
- Component selection

Trace Geometry and Impedance

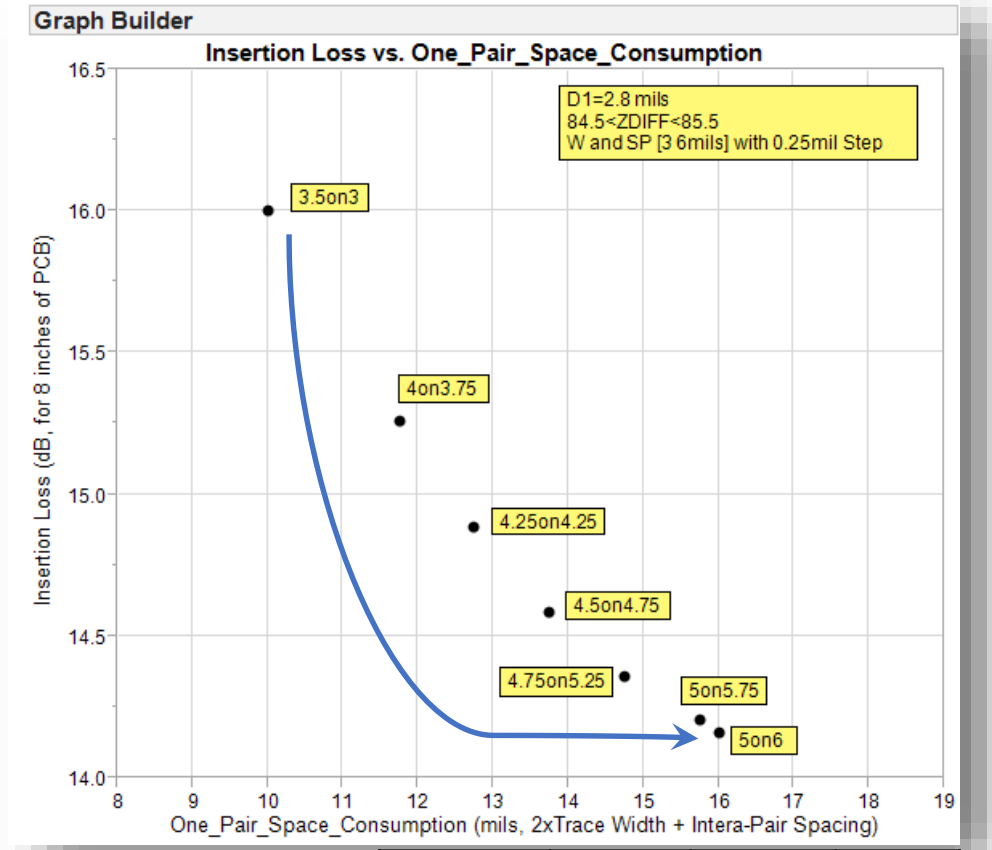
- Choose a trace geometry (width and spacing) that yields nominal differential impedance of **80-85 Ohms**
  - For short interconnects, the exact value in that range may be of importance. Recommend COM or return loss simulations to find the optimized value
  - For long channels, the exact impedance in the range is not that important. Trace loss/attenuation should become the primary design concern
- Consider the variation of impedance when assessing your design. This is important for short interconnects
  - Example: notice the impact of impedance variation on return loss and on COM



	COM
Target Zdiff – 10%	Baseline - 0.4dB
Target Zdiff	Baseline
Target Zdiff + 10%	Baseline - 1dB

Trace Geometry and Loss/Attenuation

- If your objective is long reach, reduce the attenuation of traces by optimizing the trace geometry
- The PCB vendor's recommended minimum trace width/spacing likely have not optimized loss
  - **Design Tip:** you can spend more area (i.e. larger trace width and/or spacing) to reduce loss.
- Example: for 8" of microstrip trace, the differential loss can be cut from 16dB @ 10GHz to ~14dB by optimizing the trace width/spacing from 3.5/3 mils to 5/6 mils
- Consider the variation of loss when assessing your design. See the table for an example
  - Note that aside from manufacturing variations, temperature and humidity can impact attenuation of traces



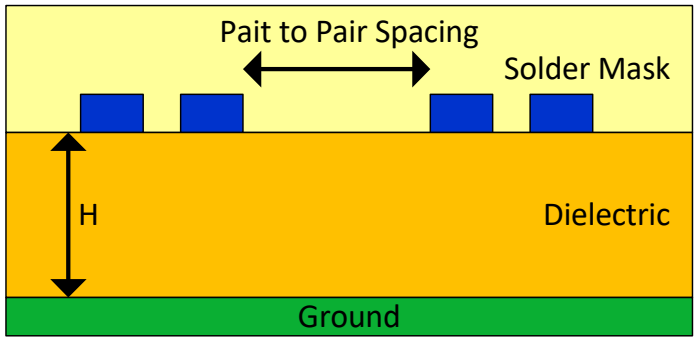
Loss at 10GHz/Length	2"	4"	6"	8"
Minimum Loss	3.4 dB	6.6	9.1	11.7
Typical Loss	4 dB	7.6	10.9	13.9
Maximum Loss	4.8 dB	8.9	12.2	16.4

Simulations data based on variation due to manufacturing and environmental conditions, not measurement

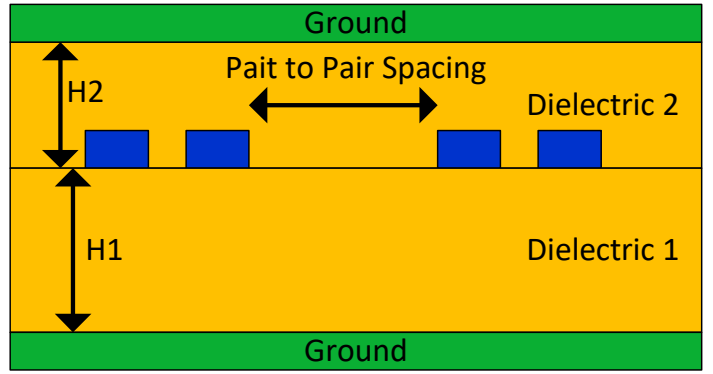
Trace Geometry and Cross Talk

- Pair-to-pair spacing (P2PS) modulates the cross talk contribution from the traces.
  - Let us define pair-to-pair spacing as a multiple of dielectric height. Example, P2PS=20xH (for stripline, H = min (H1, H2))

Microstrip



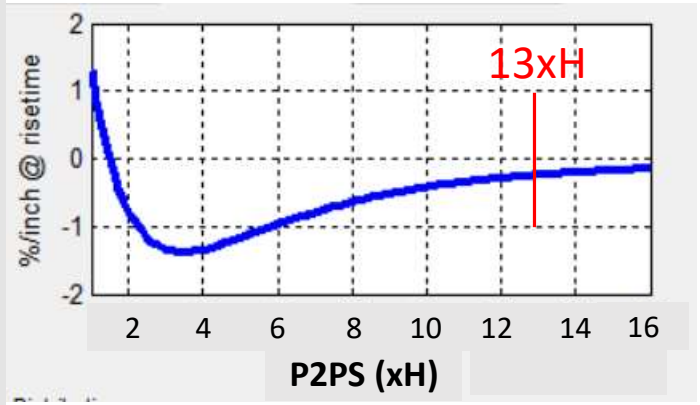
Stripline



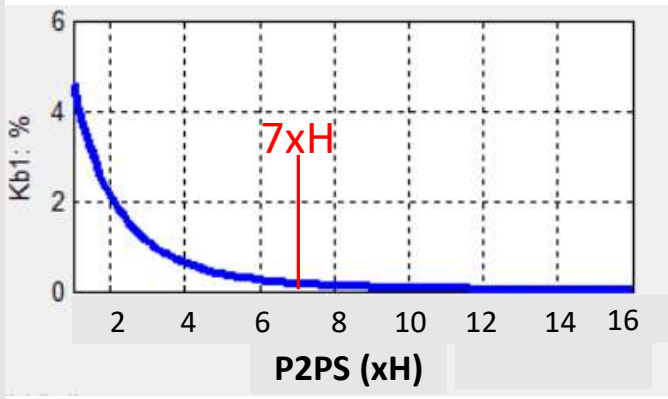
- To minimize the trace cross talk to a small level, consider the following rough guidelines

	Spacing where Cross-talk reduces significantly
Microstrip, far-end cross talk	> ~13xH
Microstrip, near-end cross talk	> ~7xH
stripline, near-end cross talk	> ~4xH

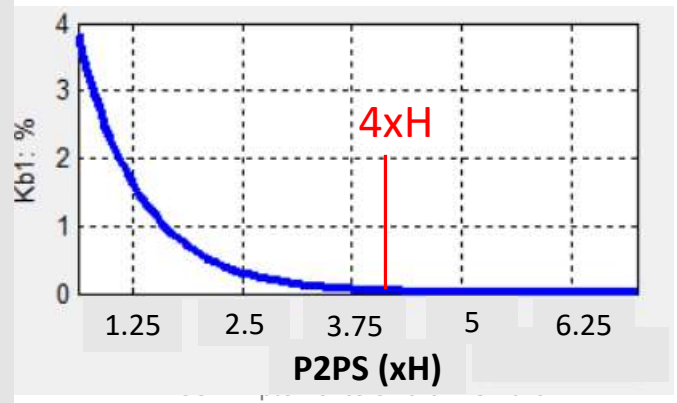
Microstrip Far-end Cross Talk



Microstrip Near-end Cross Talk



Stripline Near-end Cross Talk



USB4™ System Design Guidelines

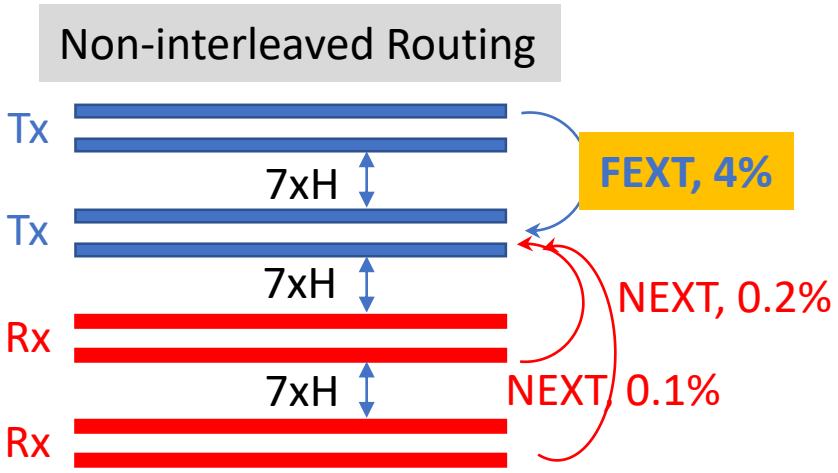
- Electrical Design Considerations
- **Physical Design Considerations**
  - Trace geometry
  - **Routing practices, vias, and component placement**
  - Layout design
- Component selection

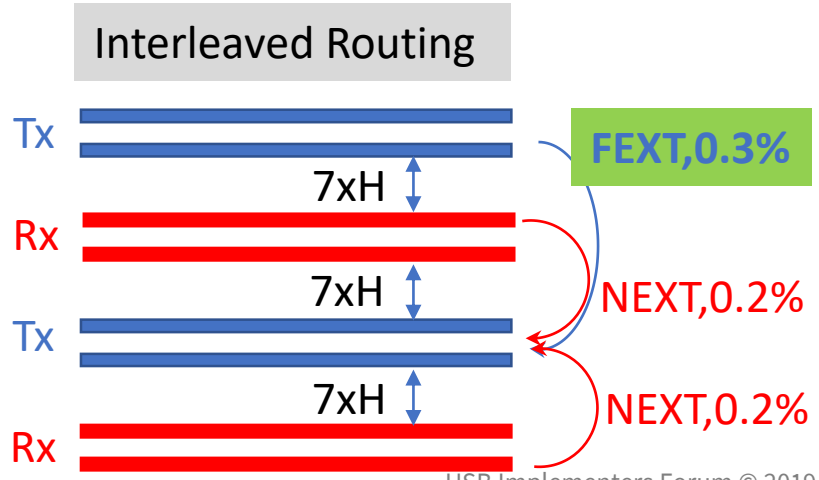
Routing on Microstrip Layer

- Routing on microstrip presents a challenge from far-end cross talk (FEXT) between two adjacent Tx or Rx pairs which increases as routing length increases
  - Example: an 8” of routing can have up to 4% FEXT when spacing is 7xH
- Mitigation options:
  - Use more than one layer to avoid placing two Tx or Rx pairs adjacent to each other
  - Use large spacing as shown in previous slide

Microstrip, far-end cross talk	Spacing > ~13xH

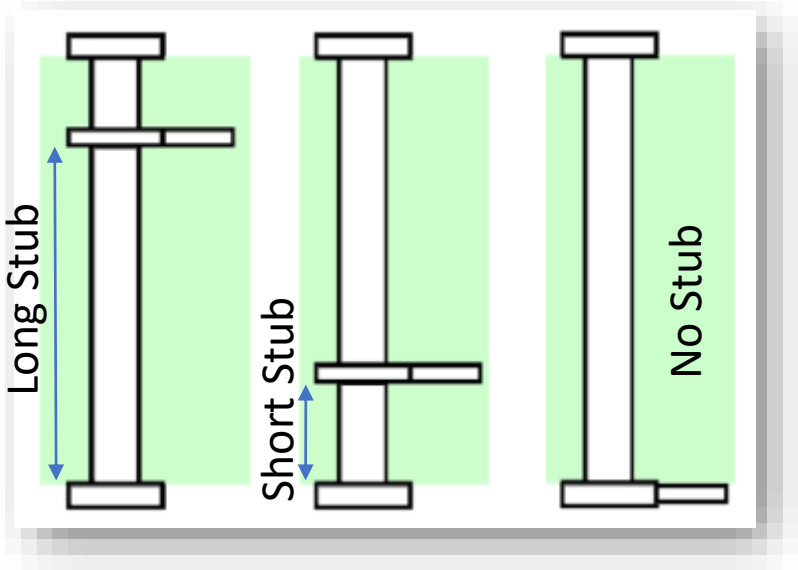
  - Consider interleaved routing, where you can increase the effective distance between two Tx or Rx without spending more board area. The trade-off is some additional near-end cross talk (NEXT)

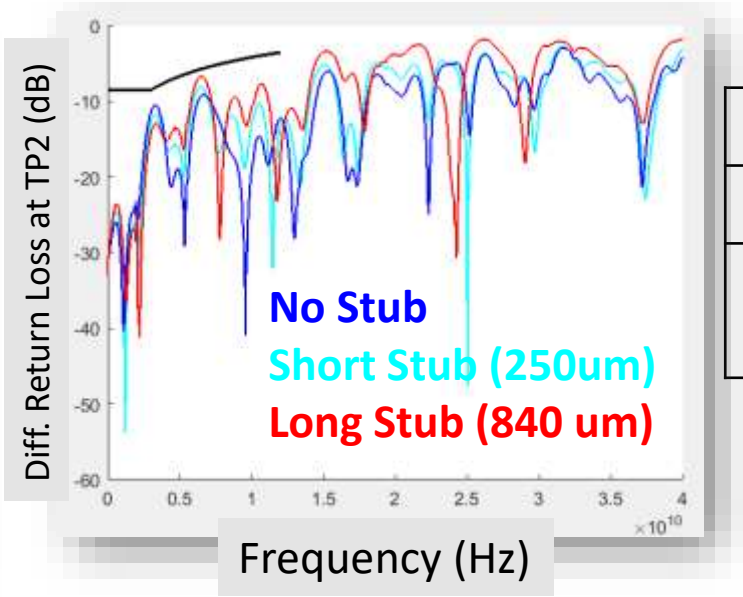




Vertical Transitions

- Avoid via stubs or minimize the length of the stub. Long stubs will negatively impact return loss, insertion loss, (hence ISI, hence DDJ), and ultimately end to end margins (e.g. COM)





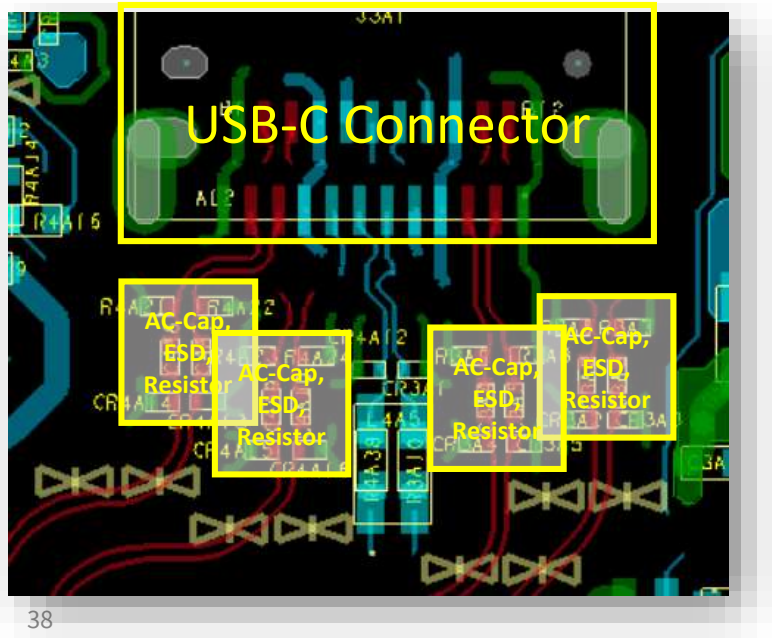
	COM
No Stub	Baseline
Short Stub(250um)	Baseline **- 0.2dB**
Long Stub (840 um)	Baseline **- 0.8dB** Failed COM

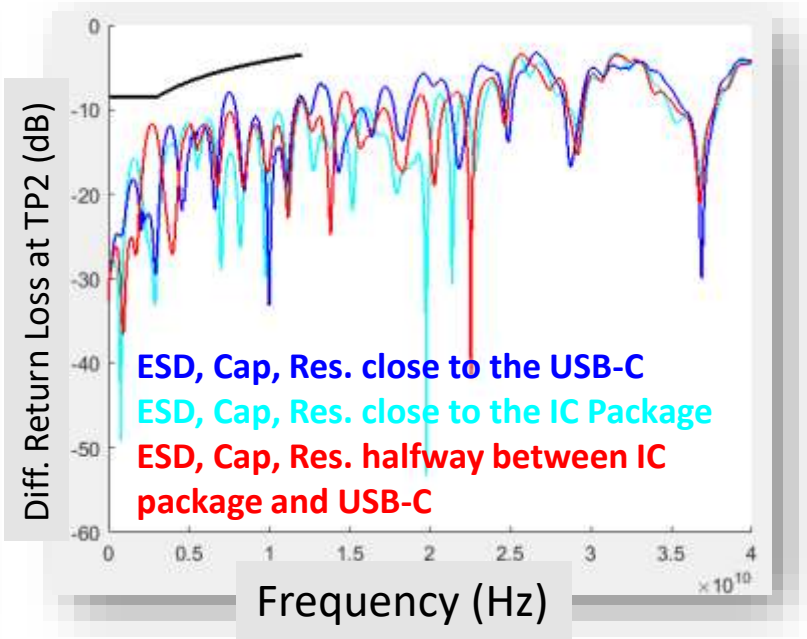
=> A long via stub will likely cause compliance and/or margin failure. Must avoid it!

- As mitigation options, consider the following
  1. Optimize impedance discontinuity by adjusting via pitch, diameter, pad/anti-pad size
  2. Other via technologies: Back-drilled via or uVia (Type-4 PCB)
  3. Routing only on surface layers
  4. If a via stub is inevitable, assess your design w/ return loss or COM simulations.

Component Placement

- Each device/components presents an impedance discontinuity because of its internal structure as well as its parasitic (e.g. its SMT pads)
- Placing as many discontinuities (devices, SMT components, vias, etc) as you can close to each other can help improve return loss (hence ISI, hence DDJ) and/or end to end margins (e.g. COM)
  - **Design Tip:** Avoid placing the ESD, ac-cap, and bleed resistors halfway between the IC package and the USB-C connector. Try to place them closer to either the IC package or the USB-C connector.





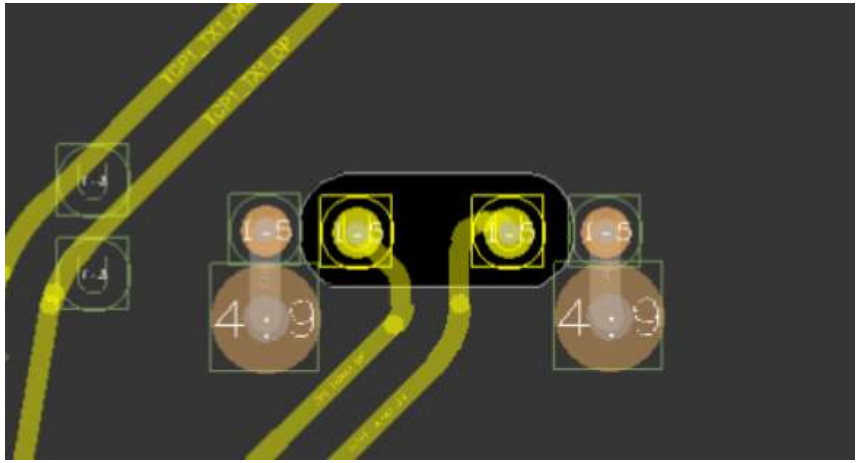
	COM
Close to USB-C	Baseline
Close to the IC PKG	Baseline **+ 1dB**
Halfway between	Baseline **- 0.9dB**

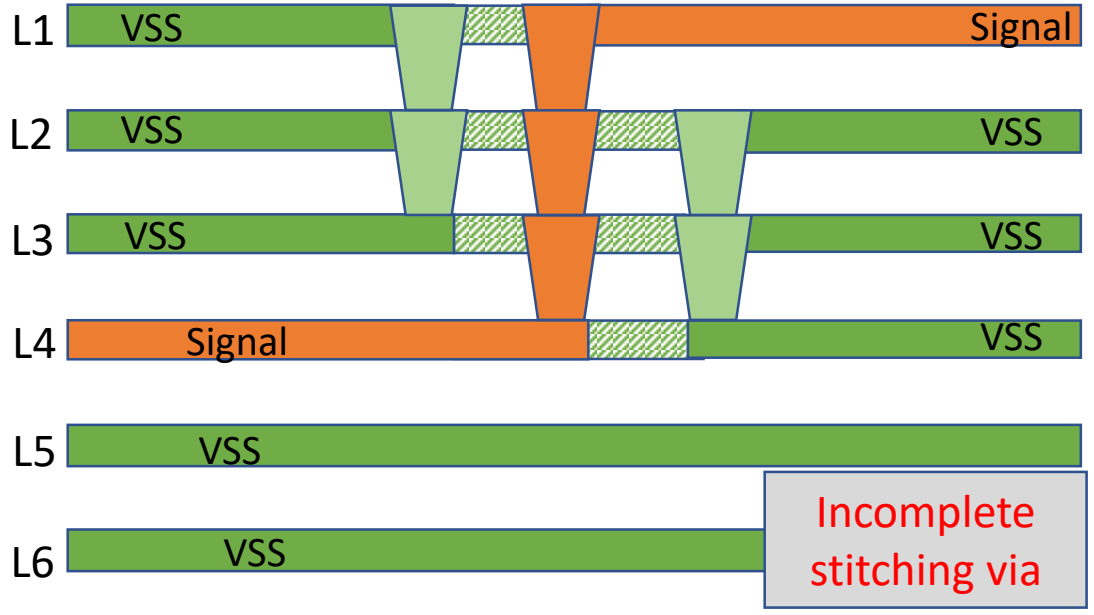
USB4™ System Design Guidelines

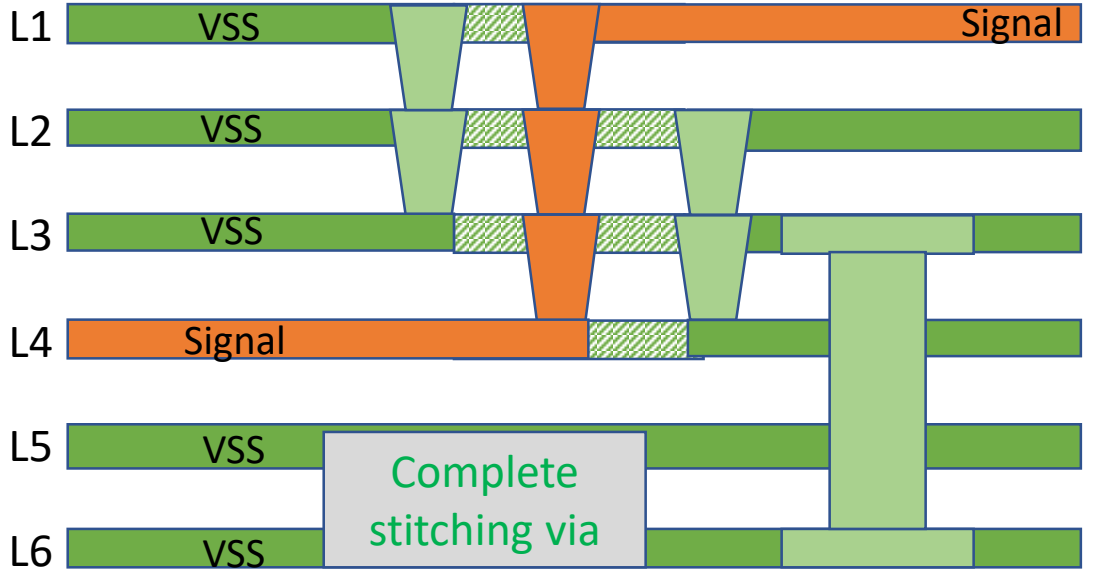
- Electrical Design Considerations
- **Physical Design Considerations**
  - Trace geometry
  - Routing practices, vias, and component placement
  - **Layout design**
- Component selection

Layout Design Guidelines - 1/7

- With signal vias, there needs to be proper stitching/return vias. For instance, a L1-L4 transition requires stitching via from L2 to L3 as well as L5 (L3 and L5 are reference planes for trace when it is routed on L4). **Pay special attention to this on Type4 PCBs**
- Symmetric placement of stitching vias is desired to minimize mode conversion

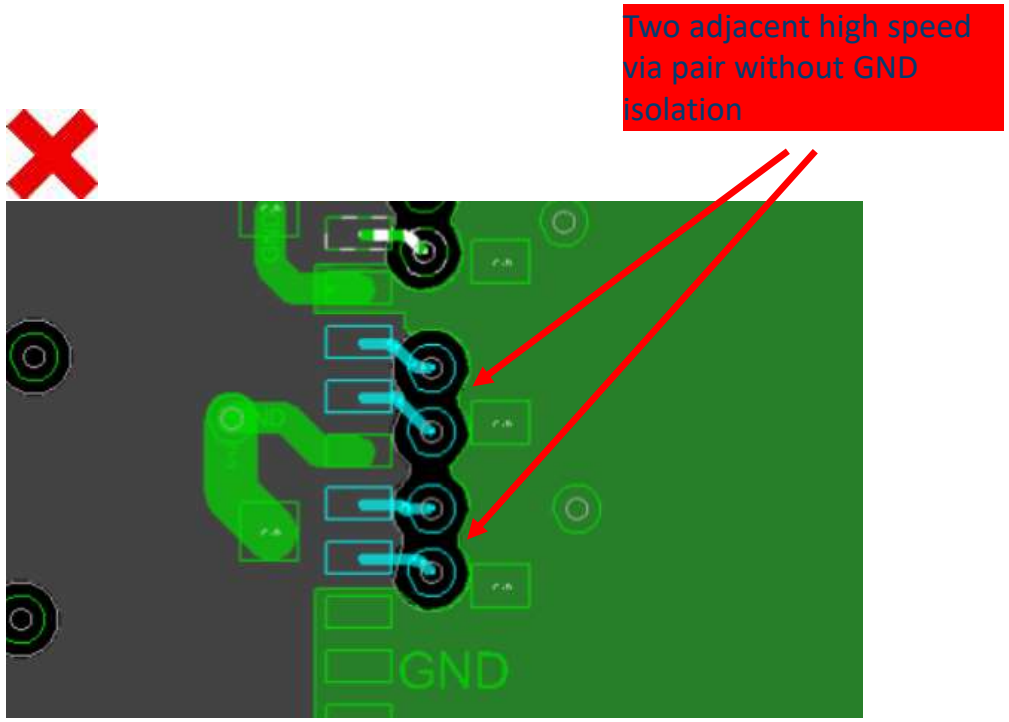


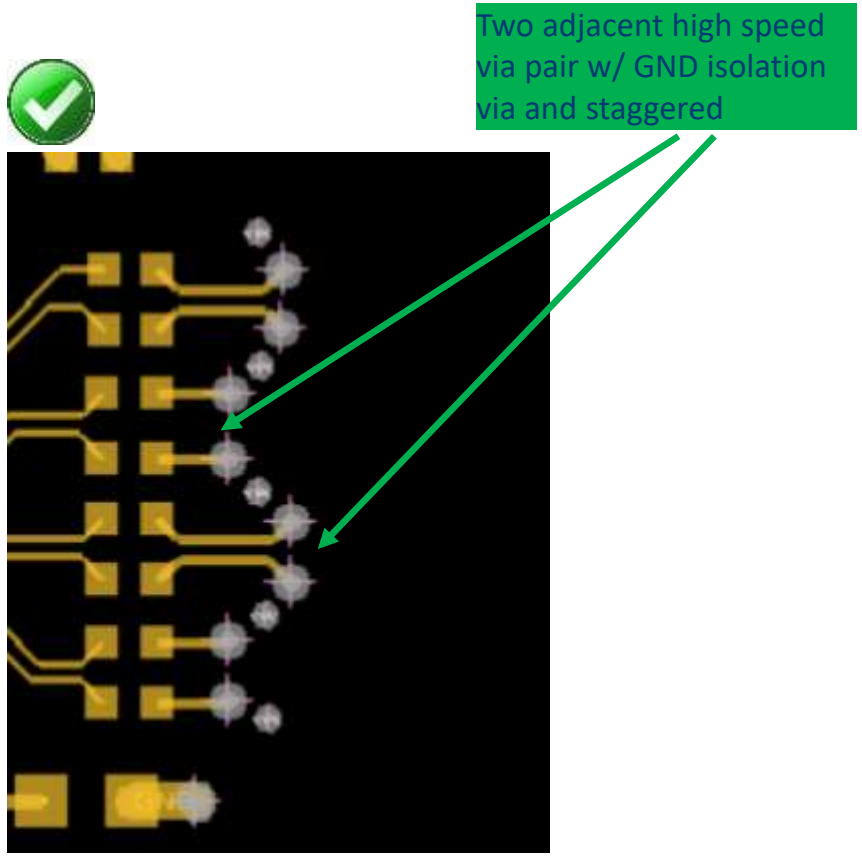




Layout Design Considerations/Examples - 2/7

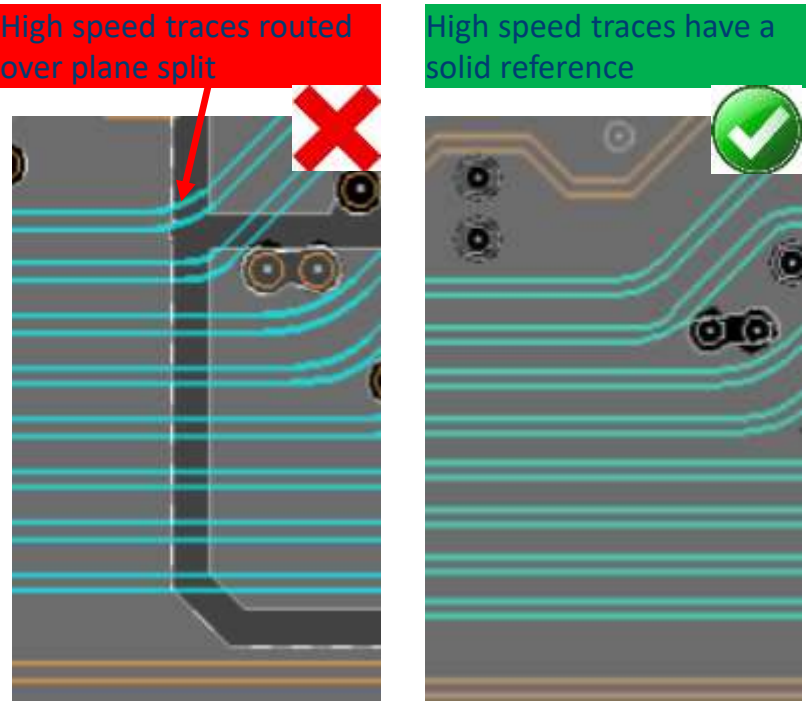
- Adjacent via pairs must be isolated with GND vias to minimize cross talk
  - Staggering the via pair left and right should provide room for placing GND via





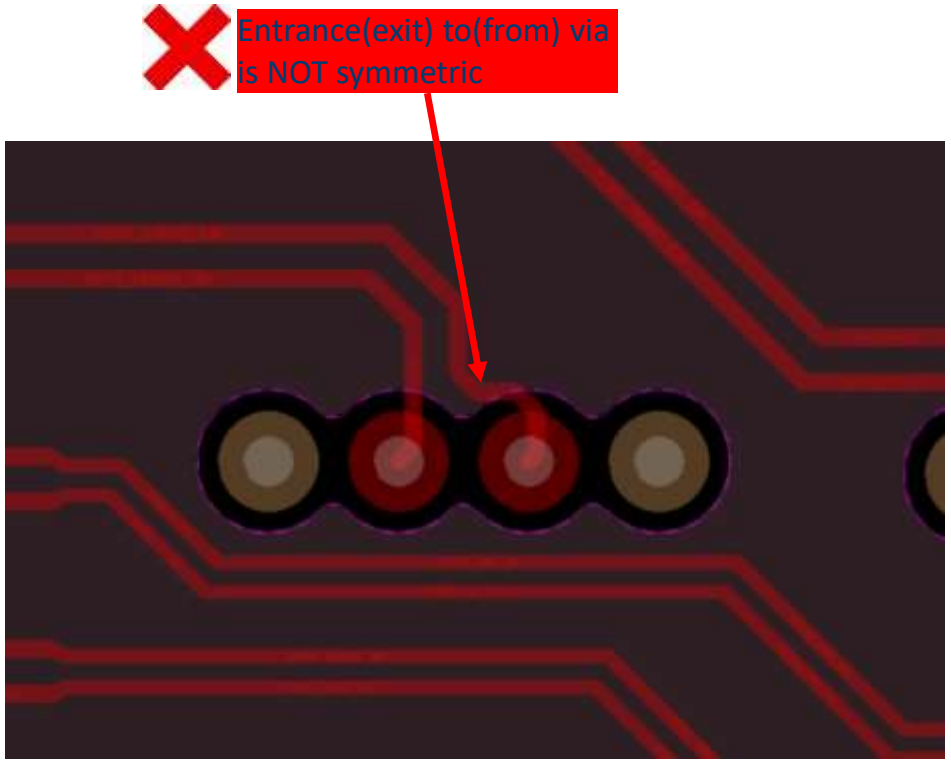
Layout Design Considerations/Examples - 3/7

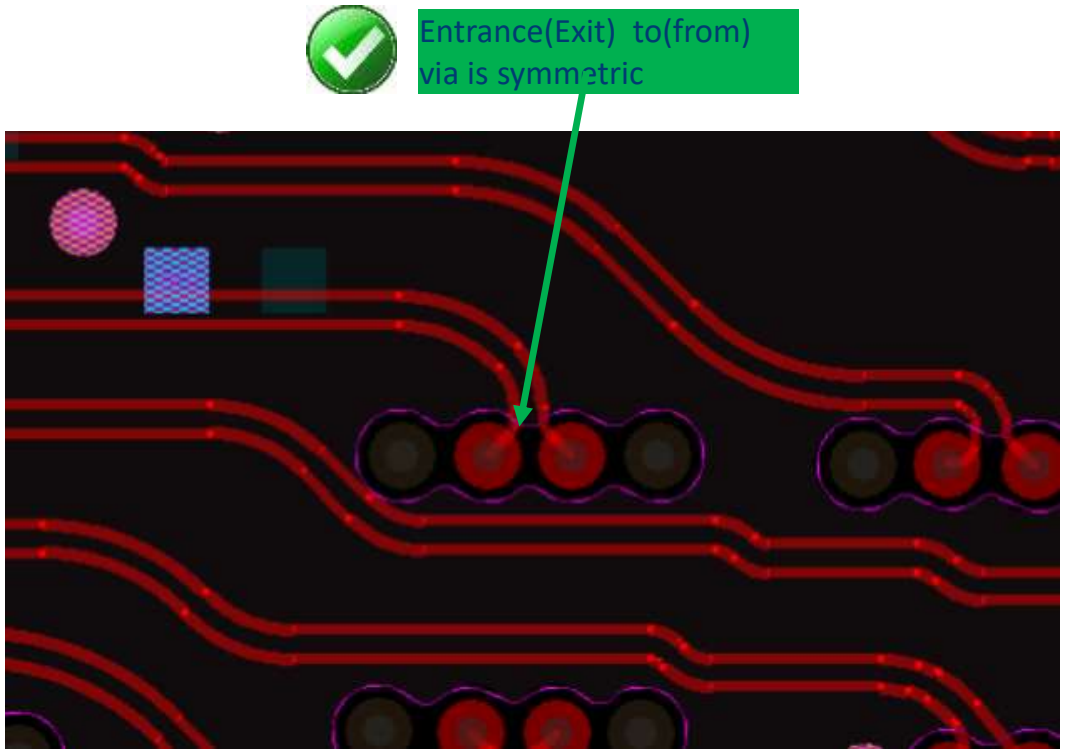
- USB4 traces should not be routed over voids or reference plane splits
  - In face, it's best to maintain a 3xH (H: height of dielectric) between trace edge and void to minimize impedance discontinuity and mode conversion



Layout Design Considerations/Examples - 4/7

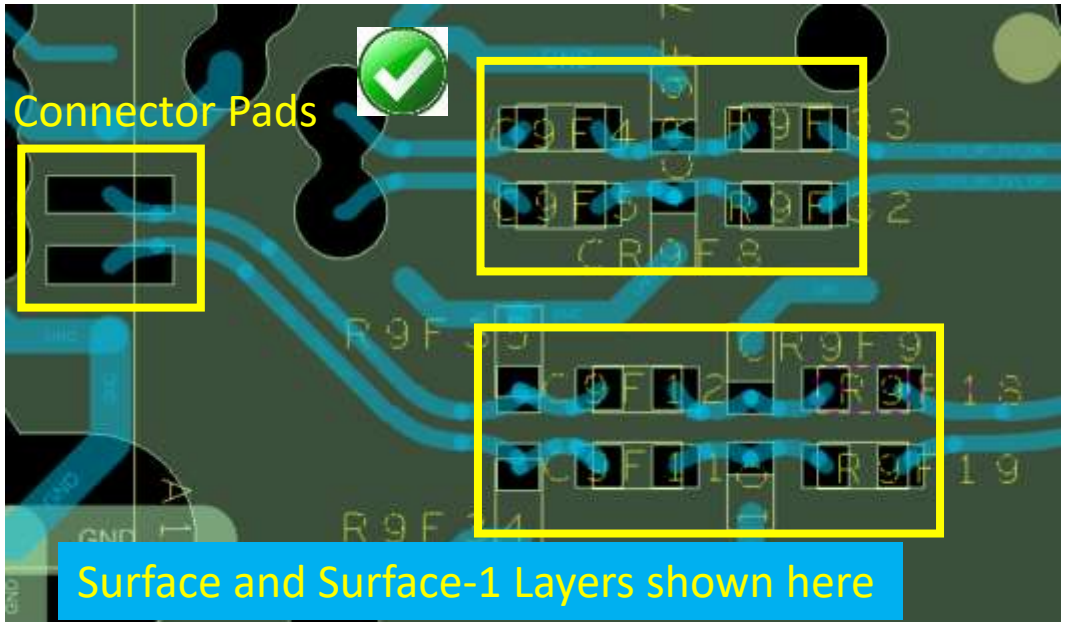
- Entrance to and exit from vias should be symmetric





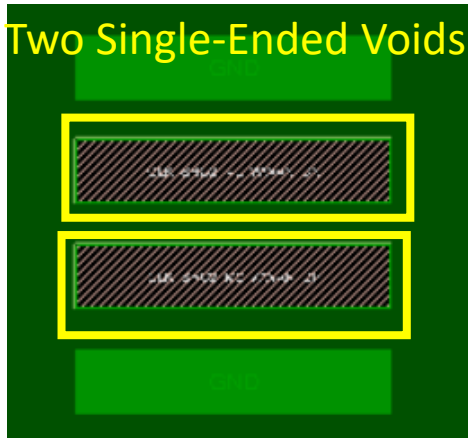
Layout Design Considerations/Examples - 5/7

- Void under SMT pads for better SI. The larger the pad size, the more important this is

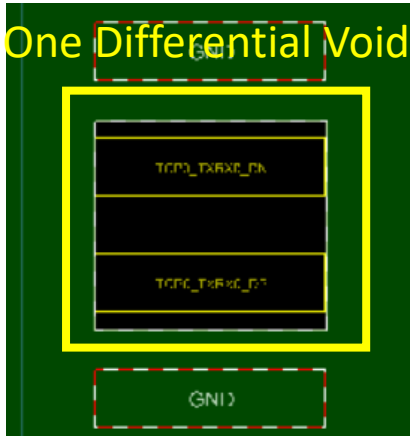


- Ensure that layer under the void (surface-2) is not a source of noise, e.g. power plane. It's best to have ground on surface-2 under the void

- **Single-ended voids** are recommended for most cases/components



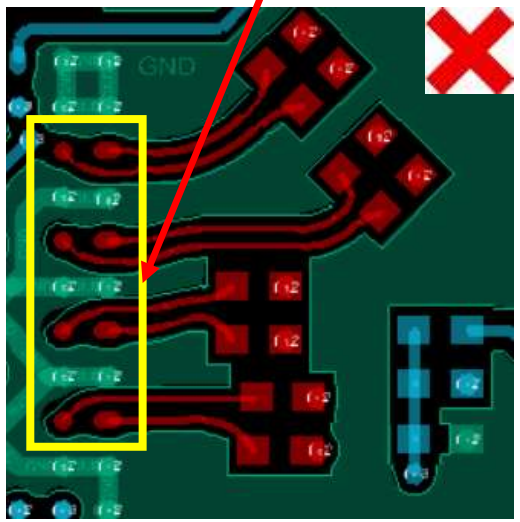
- **Differential voids** for larger pads and/or thin dielectric height (<~60um)
  - These voids can over-compensate (increase impedance too much). So analysis/3D modeling may be needed



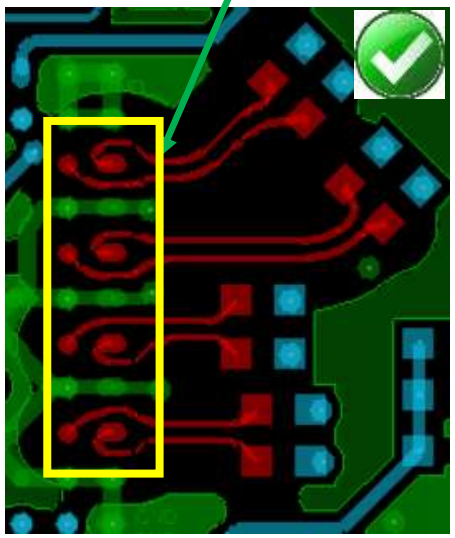
Layout Design Considerations/Examples - 6/7

- P/N length mismatch may be inevitable (due to pin out for example). Adequate P/N length matching should be considered. Any technique to achieve matching should consider the following:
  - P/N length matching should occur as close as possible to where the mismatch happens
  - Serpentine/sawtooth routing is a way to reduce P/N length mismatch, but shape of serpentine/sawtooth should be optimized

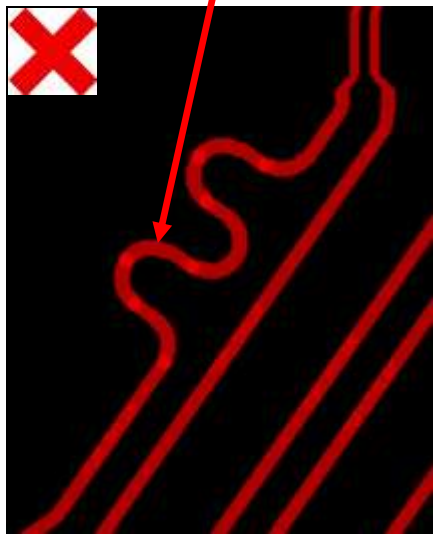
P/N length mismatch due to pin placement is not compensated



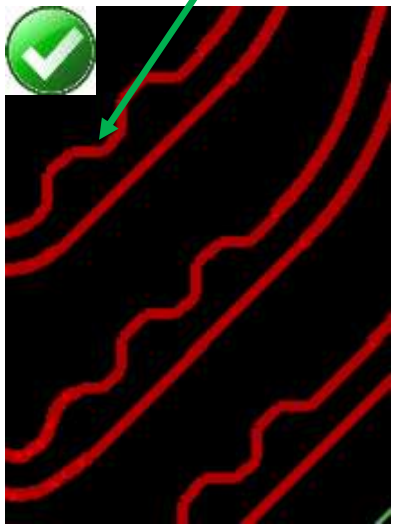
P/N length mismatch is compensated



Poorly shaped serpentine



Properly shaped serpentine/sawteeth



Layout Design Considerations/Examples - 7/7

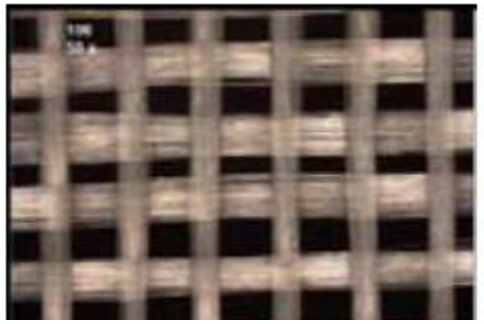
- The bends on USB4 traces should be smoothened. This should improve return loss at high frequencies

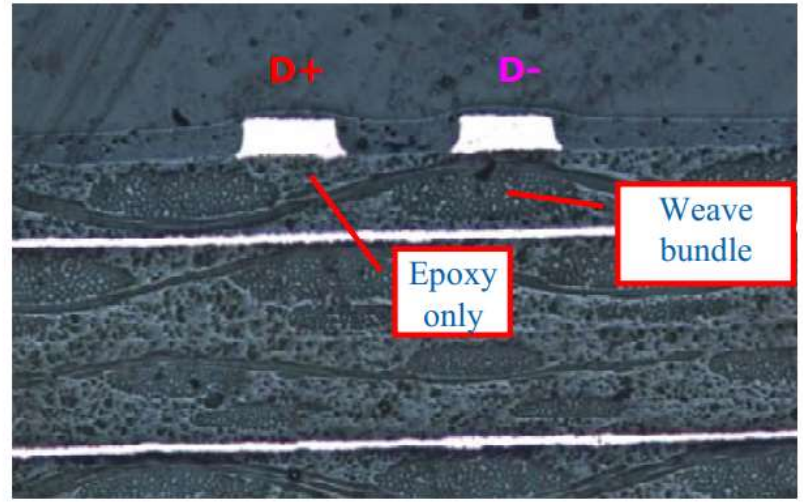
High speed traces routed with sharp bends

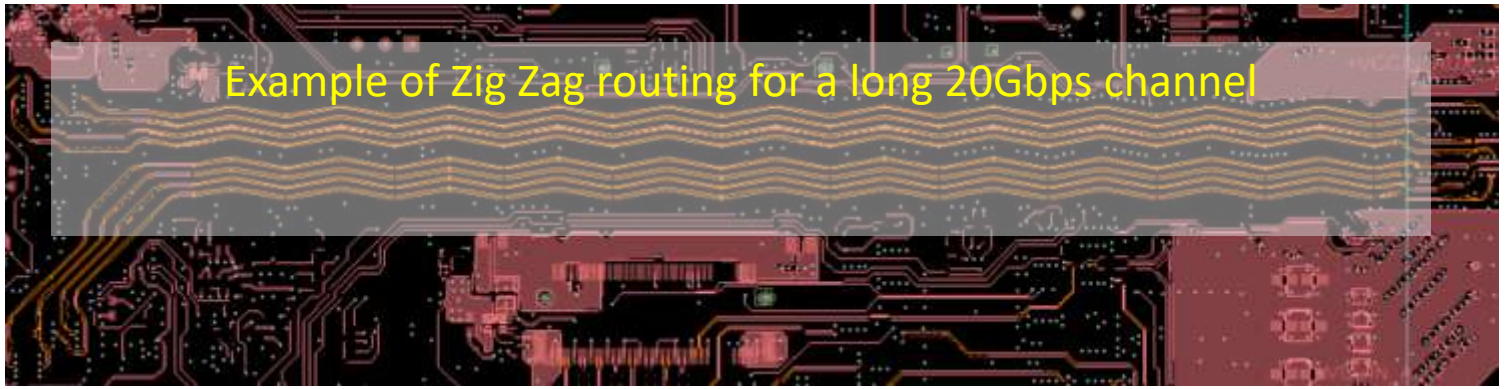
High speed signals routed with smooth bends

Fiberweave Effect

- PCBs are constructed from woven fiberglass fabric bound together with epoxy resin. The glass and epoxy have different dielectric constants.
- One half of a differential pair can run over epoxy and the other half over glass weave. Therefore, propagation delay is different between D+ and D- causing skew, which causes degraded insertion loss as well as common mode noise (i.e. mode conversion)
  - The degradation increases as the length of trace increases
- **Mitigation options are required for USB 4speeds**
- Layout mitigation techniques:
  - Angled routing
  - Zig-zag routing
  - PCB vendor rotates image of the board
  - Tighter weaves
  - Many more ….



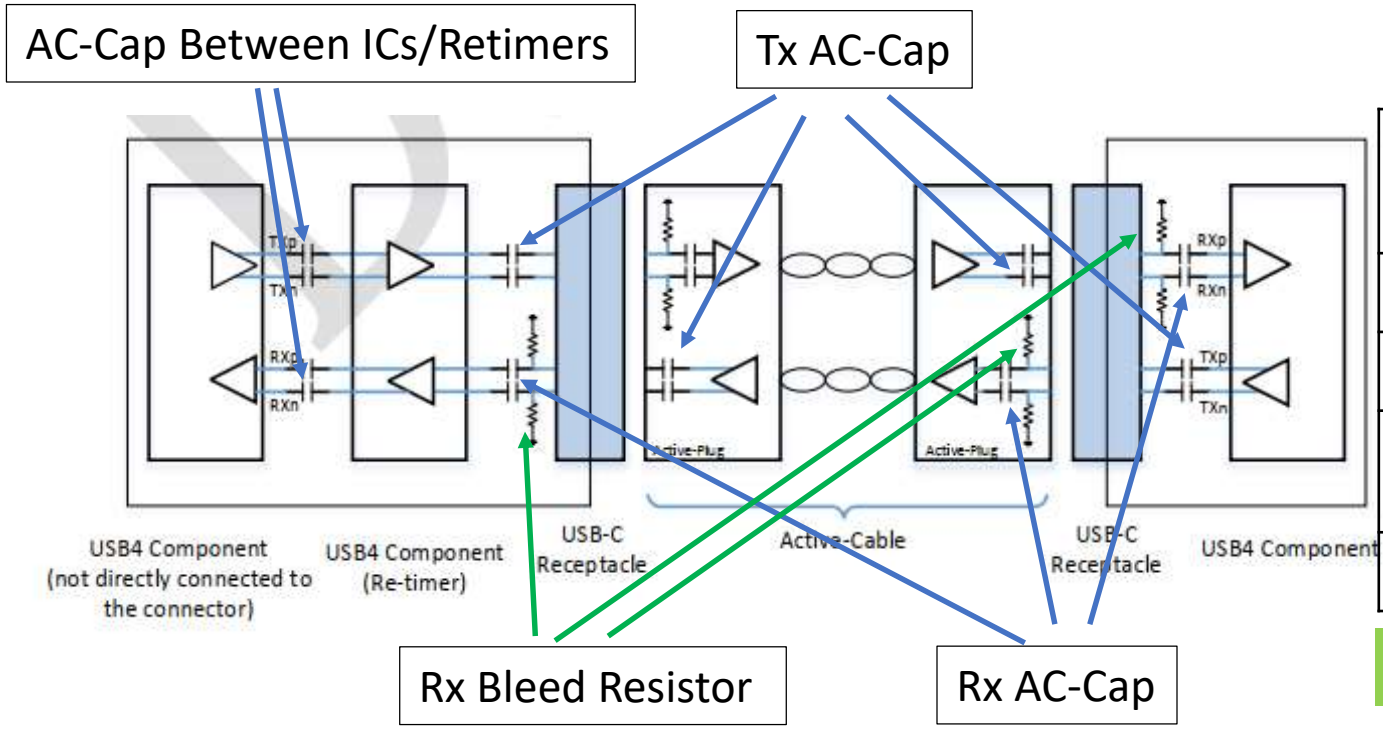




USB4™ System Design Guidelines

- Electrical Design Considerations
- Physical Design Considerations
  - Trace geometry
  - Routing practices, vias, and component placement
  - Layout design
- **Component selection**

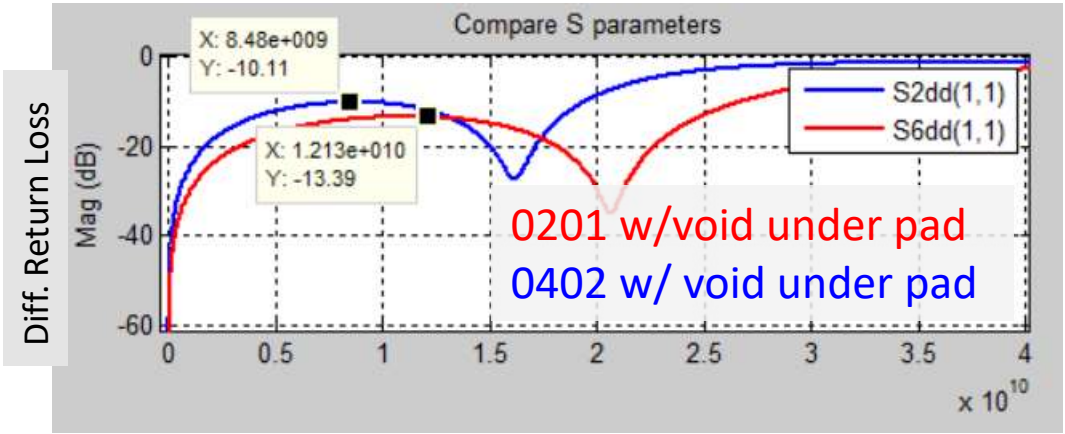
AC-Caps and Discharge Resistors



	Value	Voltage Rating	Tx	Rx
AC-Cap Between IC/Retimer	135-265nF	5V	X	X
Tx AC-Cap		25V	X	NA
Rx AC-Cap	300-363nF	25V	NA	X
Rx bleed/Discharge resistor	200-242 KΩ	25V	NA	X
Tx bleed resistor		25V	O	NA

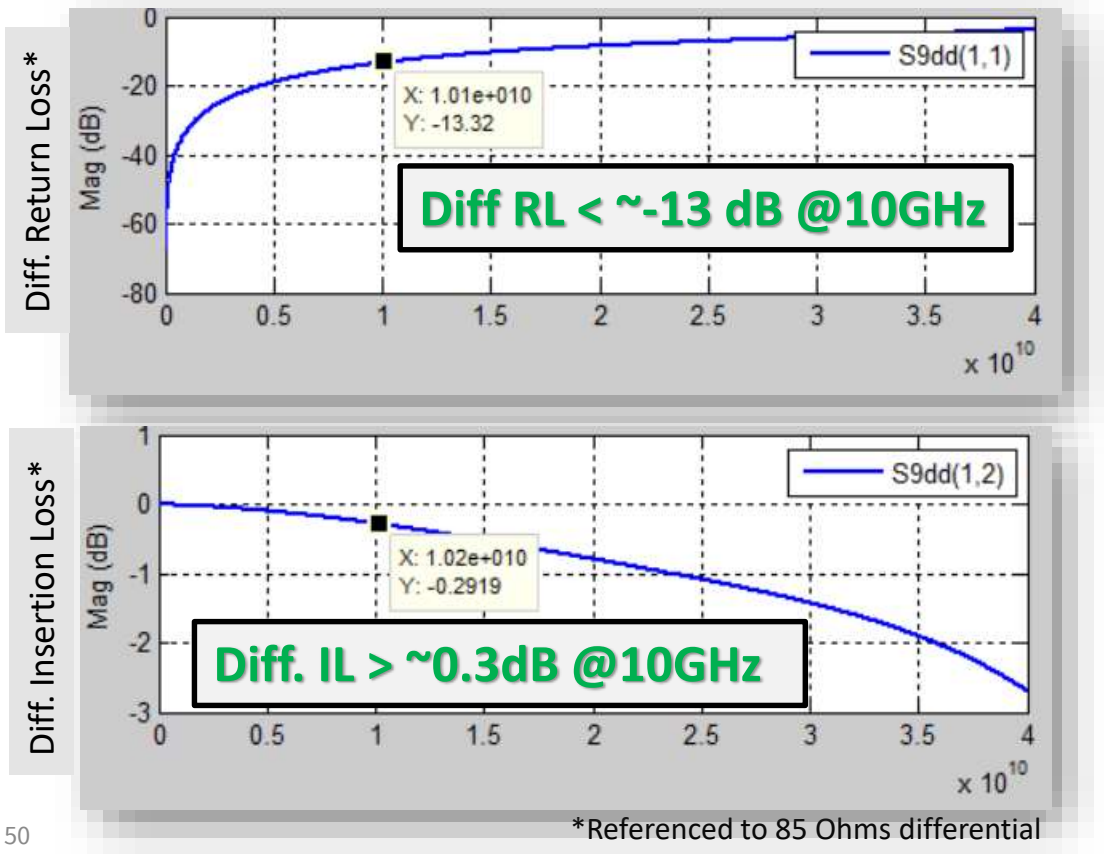
X: Mandatory O: Optional NA: Not Applicable

- Smaller size components (e.g. 0201) will have smaller parasitic and therefore better return loss than larger ones (0402). Consider using 0201 components



ESD

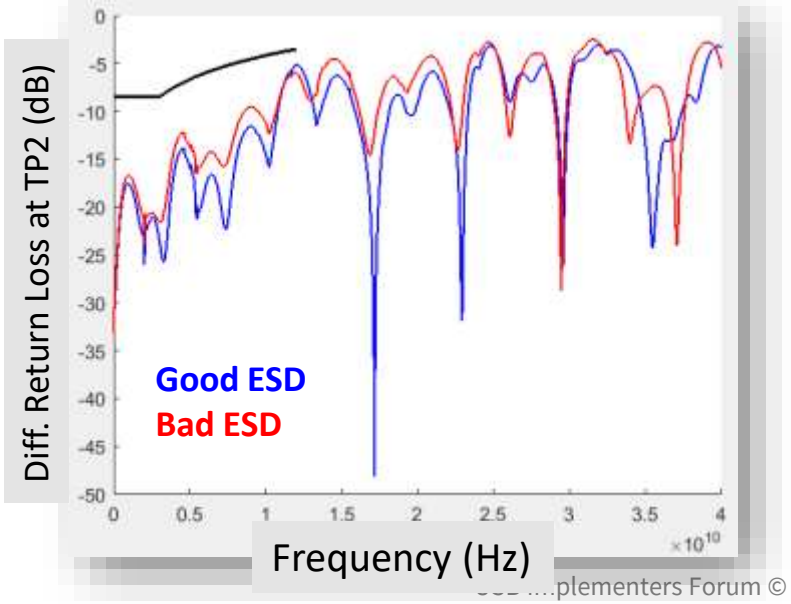
- Selection of an ESD is very important as it introduces a significant impedance discontinuity
- Recommend using an ESD whose return loss and insertion loss is similar or better than shown below:



*Referenced to 85 Ohms differential

- **Example: Impact of a poorly selected ESD**: an ESD that fails the RL guideline by ~4.3 dB and the IL by 0.4dB has a large impact to COM and degrades return loss at TP2 when used in short channel

	COM
Good ESD	Baseline
Bad ESD	Baseline - **0.9dB** => Failing COM



PCB Material

- **PCB Thickness:** The tradeoff for thinner PCBs (=>thinner dielectric) is higher trace loss
  - Example: notice the dependence of loss per inch to dielectric height for a microstrip

Dielectric height	2.7 mils	2.5	2.3
Loss @ 10GHz (dB/inch)	1.66	1.72	1.82

- **Mitigation options for reducing loss,** especially in thin PCBs:
  - PCB material and copper selection
  - Optimizing trace geometry (less effective for thin PCBs)

- **Dielectric Loss**
  - Low loss and mid loss materials can recover the interconnect reach when using a thin PCB

	Diff. Loss Per Inch
Regular loss (Df = 0.015)	1.8dB/inch
Mid loss (Df = 0.011)	1.6dB/inch
low loss (Df = 0.005)	1.2 dB/inch

Example: Stripline w/ D1/D2~=60um

- **Copper Foil Roughness**
  - At USB4 Gen 3 data rate, copper roughness impacts loss.

Loss per inch @ 10GHz	Ultra-smooth	Smooth	Less rough	Very Rough
Microstrip	1.34	1.43	1.52	1.6
Stripline (thin PCB)	1.66	1.83	2	2.16

Summary

- Two categories of channel/interconnect => different design targets/priorities
- Explicit electrical design targets per the USB4 spec
  - Loss => ISI => DDJ
  - Return loss
- Optimize trace geometry for Impedance, loss, and cross talk
- Routing practices
  - Reduce cross talk by interleaved routing
  - Avoid via stubs
  - Optimize the placement of discrete components (e.g. AC-caps, ESD, etc)
- Layout design guidelines
- Fiberweave effect and mitigation techniques
- Correct values and voltage rating of Rs and Cs
- Choose an ESD with better or equal to the recommended electrical performance
- PCB dielectric material and copper has large impact on trace loss at USB4 data rates

Time for Q&A